Performance Characteristics:

- Working mode: The input pulse signal is converted to the complementary signal output
- Operating voltage: -5V
- Input level: Compatible with TTL level
- Output level: 0/-5V
- Static current: 2mA
- Chip size: 2.1mm x 1.13mm x 0.1mm

Product Description:

CW-FEN6 is a 6-bit FET driver chip, manufactured by GaAs process, which can generate 0V/-5V complementar y pulse output from the input TTL pulse signal.The chip size is 2.1mm×1.13mm×0.1mm.

Electrical parameters: (T_A=+25℃,VEE=-5V)

Parameter name	Symbols	Minimum	Typical	Maximum	Units	Instructions
Power supply voltage	V_{EE}	-5.5	-5	-4.5	V	Normal operating
Static current	I_{EE}	-	2	-	mA	Current after the chip
Input high level	V_{IH}	2.8	5	5	V	Input voltage of pin
Input low level	V_{IL}	0	0	0.4	V	A1-A6, compatible
Input current	I_i	-	0.4	-	mA	-
Output high level	V_{OH}	-	0	-	V	In-phase and
Output low	V_{OL}	-	-5	-	V	antiphase ends (1A,
Output (drive) current	Io	-	2	-	mA	Related to load
Operating frequency	f	0	10	30	MHz	Load dependent
Switching time	t	-	16	25	ns	-
Temperature	T_A	-55	25	85	℃	-

Use limit parameters: (Exceeding any of the following maximum limits risks permanent damage)

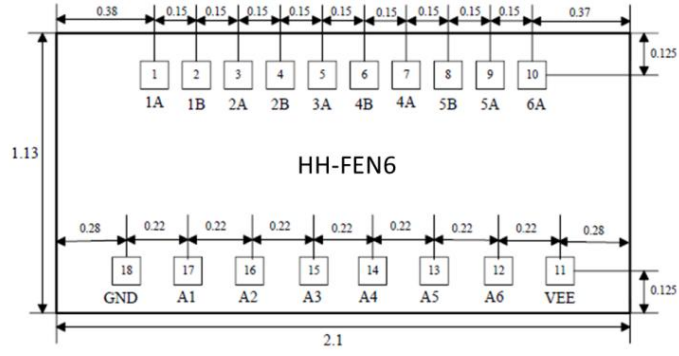
Power supply voltage	-6V
Input high level	5.5V
Input low	-0.5V
Storage temperature	-65℃~+150℃

Truth table:

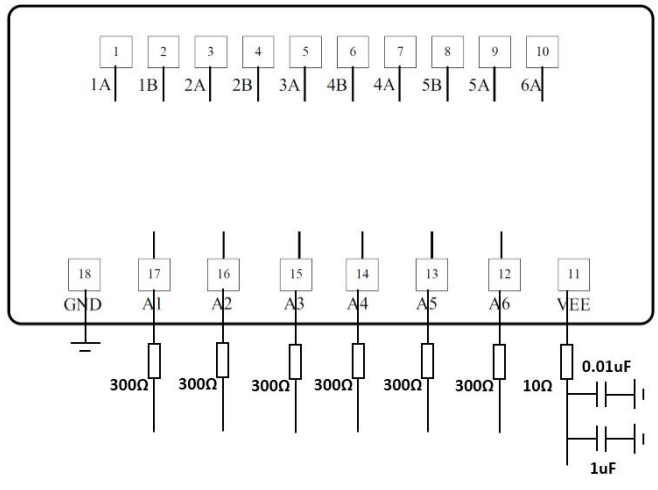
Input						Output									
A1	A2	A3	A4	A5	A6	1A	1B	2A	2B	3A	4B	4A	5B	5A	6A
Li	Li	Li	Li	Li	Li	Lo	Ho	Lo	Ho	Lo	Ho	Lo	Ho	Lo	Lo
Hi	Li	Li	Li	Li	Li	**Ho**	**Lo**	Lo	Ho	Lo	Ho	Lo	Ho	Lo	Lo
Li	**Hi**	Li	Li	Li	Li	Lo	Ho	**Ho**	**Lo**	Lo	Ho	Lo	Ho	Lo	Lo
Li	Li	**Hi**	Li	Li	Li	Lo	Ho	Lo	Ho	**Ho**	Ho	Lo	Ho	Lo	Lo
Li	Li	Li	**Hi**	Li	Li	Lo	Ho	Lo	Ho	Lo	**Lo**	**Ho**	Ho	Lo	Lo
Li	Li	Li	Li	**Hi**	Li	Lo	Ho	Lo	Ho	Lo	Ho	Lo	**Lo**	**Ho**	Lo
Li	Li	Li	Li	Li	**Hi**	Lo	Ho	Lo	Ho	Lo	Ho	Lo	Ho	Lo	**Ho**
Hi	Hi	Hi	Hi	Hi	Hi	Ho	Lo	Ho	Lo	Ho	Lo	Ho	Lo	Ho	Ho

Note: Take the input pulse level of 0/5V and the supply voltage of -5V, L_iRepresents 0V, H_iRepresents 5V, L_oIt means -5V, H_oRepresents 0V.

Size drawing: (unit mm)



Suggested assembly drawing:



Instructions:

Working conditions: The input end should be connected in series with 300Ω ~ 3ω protection resistance, under the premise of meeting the switching speed, the larger the protection resistance, the better.

Storage: The chip must be placed in a container with electrostatic protection function, and stored in a nitrogen environment.

Cleaning treatment: The bare chip must be operated and used in a purified environment. It is forbidden to use liquid cleaning agent to clean the chip.

Electrostatic protection: Strictly comply with the ESD protection requirements to avoid electrostatic damage to the components.

General operation: Use vacuum chuck or precision pointed tweezers to pick up the chip.Avoid touching the surface of the chip with tools or fingers during handling.

Mounting operation: The chip can be installed using AuSn solder eutectic welding or conductive adhesive bonding process.The mounting surface must be clean and flat.

Bonding operation: Input and output with 2 (recommended diameter of 25um gold wire) bonding wire, bonding wire length less than 250um is optimal.It is recommended to use the smallest possible ultrasonic energy.Bonding begins at the pressure point on the chip and ends at the package (or substrate).