Performance Characteristics:

- Working mode: The input pulse signal is converted to the complementary signal output
- Operating voltage: -5V
- Input level: Compatible with TTL level
- Output level: 0/-5V
- Static current: 2mA
- Chip size: 2.1mm x 1.13mm x 0.1mm

Product Description:

CW-FEN6B is a 6-bit FET driver chip, manufactured by GaAs process, which can generate 0V/-5V complement ary pulse output from the input TTL pulse signal.

Electrical parameters: (T_A=25℃)

Parameter	Symbols	Minimum	Typical value	Maximum	Units	Instructions
Power supply	V_{EE}	-5.5	-5	-4.5	V	Chip operating
Static current	I_{EE}	-	2	-	mA	Current after
Input high	V_{IH}	2.8	5	5	V	A1-A6 input voltage is
Input low	V_{IL}	0	0	0.4	V	
Input current	I_i	-	0.4	-	mA	-
Output high	V_{OH}	-	0	-	V	The output voltage of the
Output low	V_{OL}	-	-5	-	V	
Output	Io	-	2	-	mA	Load
Operating	F	0	10	30	MHz	Load
Switching	t	-	14	25	ns	-
Temperature	Ta	-55	25	85	℃	-

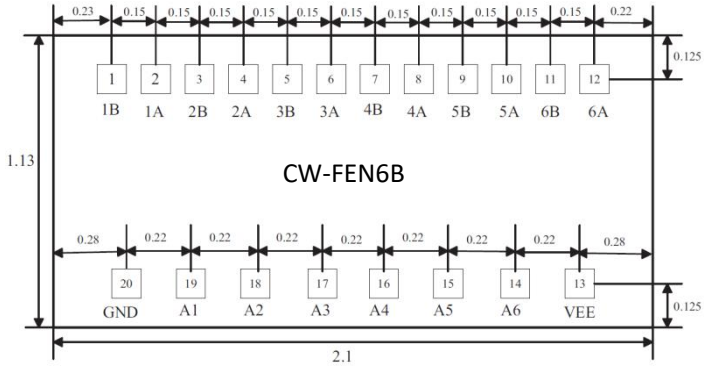
Use limit parameters: (Exceeding any of the following maximum limits risks permanent damage)

Power supply voltage	-6V
Input high level	5.5V
Input low	-0.5V
Storage temperature	-65℃~+150℃

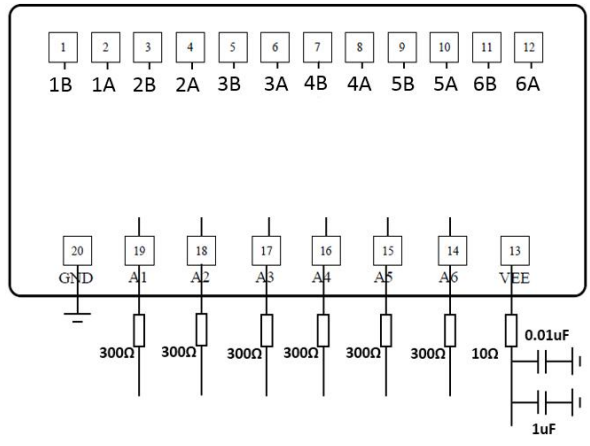
Truth table: (unit: V)

Input						Output											
A1	A2	A3	A4	A5	A6	1A	1B	2A	2B	3A	3B	4A	4B	5A	5B	6A	6B
0	0	0	0	0	0	-5	0	-5	0	-5	0	-5	0	-5	0	-5	0
5	0	0	0	0	0	**0**	**-5**	-5	0	-5	0	-5	0	-5	0	-5	0
0	**5**	0	0	0	0	-5	0	**0**	**-5**	-5	0	-5	0	-5	0	-5	0
0	0	**5**	0	0	0	-5	0	-5	0	**0**	**-5**	-5	0	-5	0	-5	0
0	0	0	**5**	0	0	-5	0	-5	0	-5	0	**0**	**-5**	-5	0	-5	0
0	0	0	0	**5**	0	-5	0	-5	0	-5	0	-5	0	**0**	**-5**	-5	0
0	0	0	0	0	**5**	-5	0	-5	0	-5	0	-5	0	-5	0	**0**	**-5**
5	5	5	5	5	5	0	-5	0	-5	0	-5	0	-5	0	-5	0	-5

Size drawing: (unit mm)



Suggested assembly drawing:



Instructions:

Working conditions: The input end should be connected in series with 300Ω ~ 3ω protection resistance, under the premise of meeting the switching speed, the larger the protection resistance, the better.

Storage: The chip must be placed in a container with electrostatic protection function, and stored in a nitrogen environment.

Cleaning treatment: The bare chip must be operated and used in a purified environment. It is forbidden to use liquid cleaning agent to clean the chip.

Electrostatic protection: Strictly comply with the ESD protection requirements to avoid electrostatic damage to the components.

General operation: Use vacuum chuck or precision pointed tweezers to pick up the chip.Avoid touching the surface of the chip with tools or fingers during handling.

Mounting operation: The chip can be installed using AuSn solder eutectic welding or conductive adhesive bonding process.The mounting surface must be clean and flat.

Bonding operation: Input and output with 2 (recommended diameter of 25um gold wire) bonding wire, bonding wire length less than 250um is optimal.It is recommended to use the smallest possible ultrasonic energy.Bonding begins at the pressure point on the chip and ends at the package (or substrate).