Performance Characteristics:

- Frequency band: 2~20GHz
- Isolation: 38dB
- Insertion loss: 3.0dB
- Enter P1dB: 16dBm
- Input standing wave (open state) : 1.6
- Output standing wave (open state) : 1.8
- VEE=-5V, A1/A2, mirror B1/B2 different power supply switching switch path
- Chip size: 1.5mm x 1.55mm x 0.1mm

Product Description:

The CW-SW30220 is a GaAs MMIC band control single-pole three-throw switch chip with a frequency range covering 2 to 20 GHZ and an entire band insertion loss of less than 3.0dB.Adopt VEE=-5V, A1/A2, mirror B1/B2 different power supply switching switch path.

Electrical parameters: (TA=25℃, VEE=-5V)

Indicators	Minimum	Typical value	Maximum value	Units
Frequency range	2~20			GHz
Insertion loss	-	-	3.0	dB
isolation	38	-	-	dB
Input standing wave (open state)	-	-	1.6	-
Output standing wave (open state)	-	-	1.8	-
Enter P1dB	16	-	-	dBm

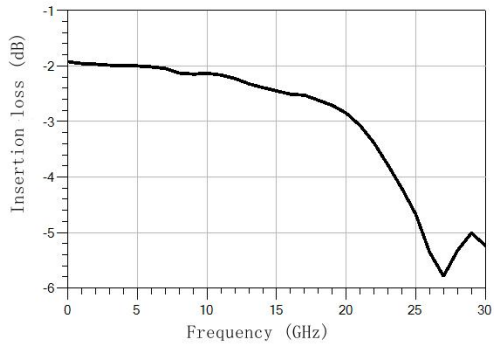
Use limiting parameters:

Input power	+20dBm
Storage temperature	-65℃~150℃
Service temperature	-55℃~85℃

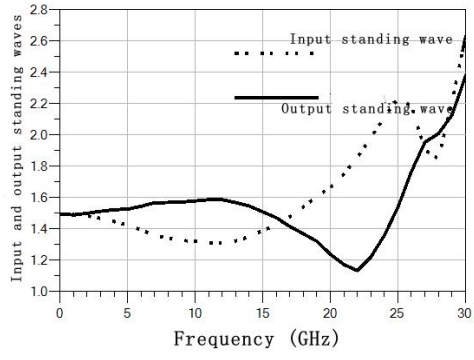
Typical curves (not mirrored):

OUT1-ON

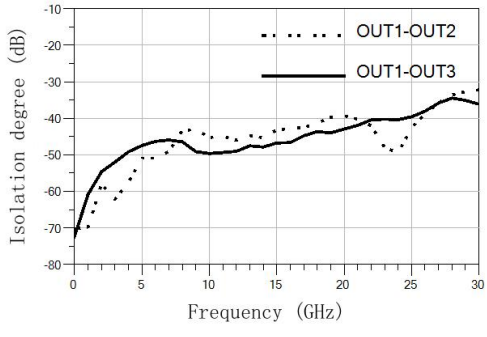
Insert loss



I/O standing wave

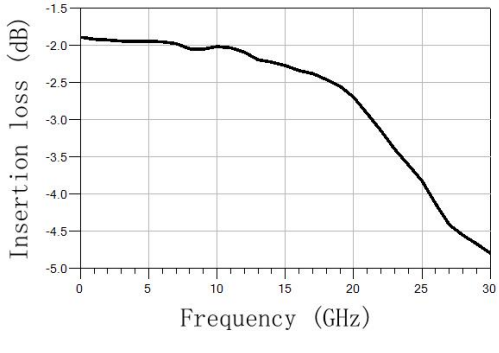


isolation

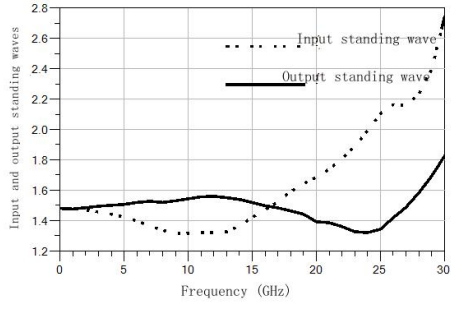


OUT2-ON

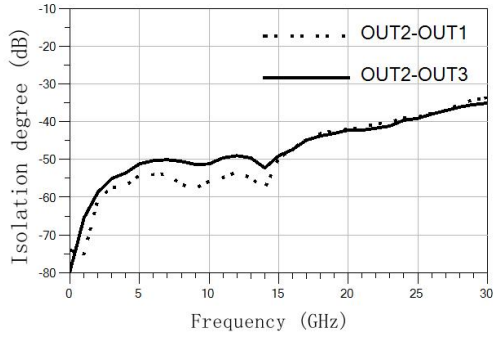
Insert loss



I/O standing wave

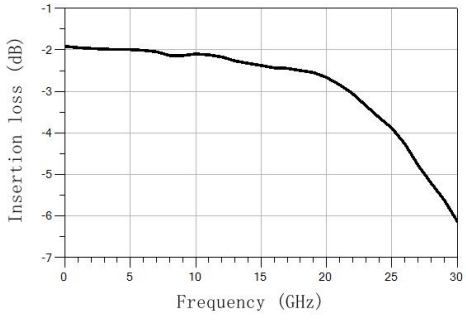


isolation

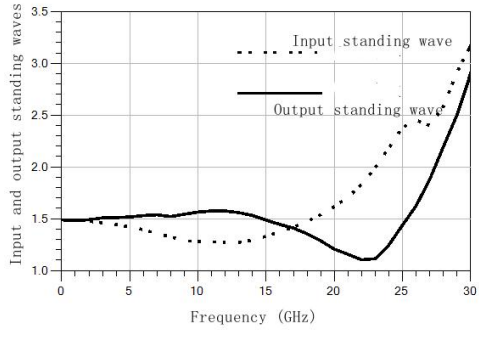


OUT3-ON

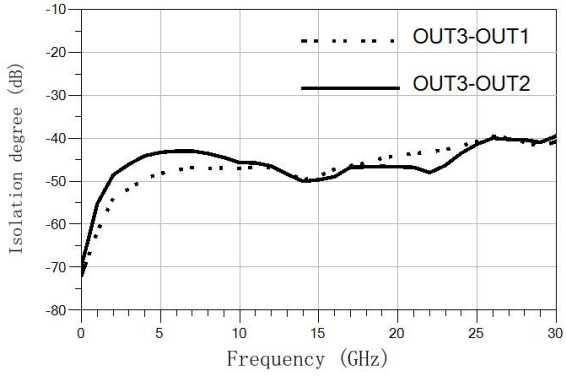
Insertion loss



I/O standing wave



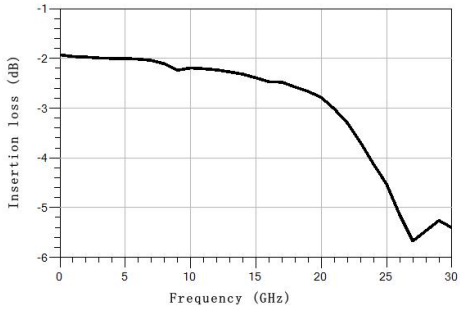
isolation



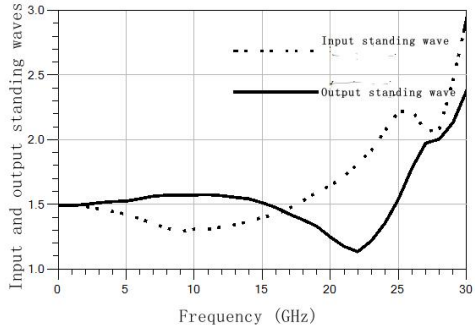
Typical curve (mirror image):

OUT1-ON

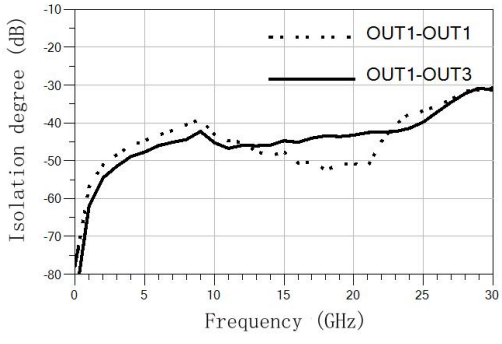
Insert loss



I/O standing wave

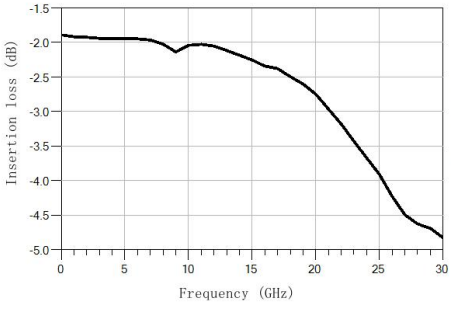


isolation

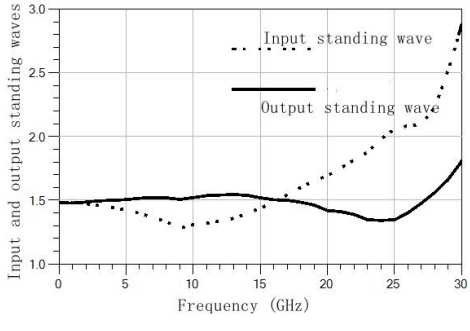


OUT2-ON

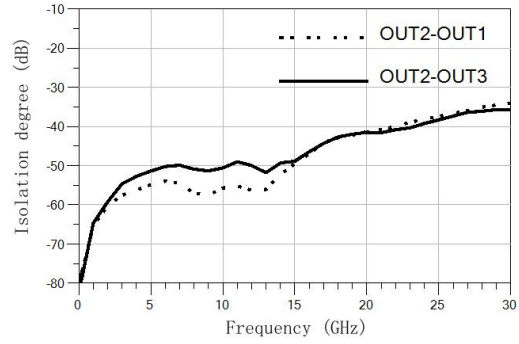
Insert loss



I/O standing wave

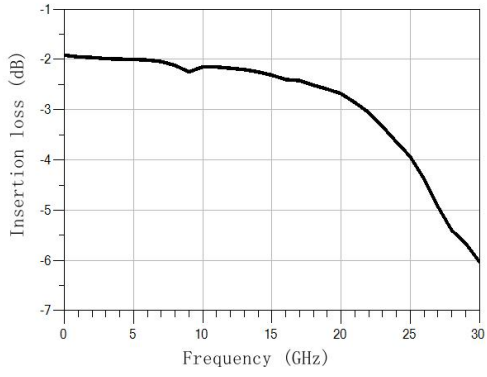


isolation

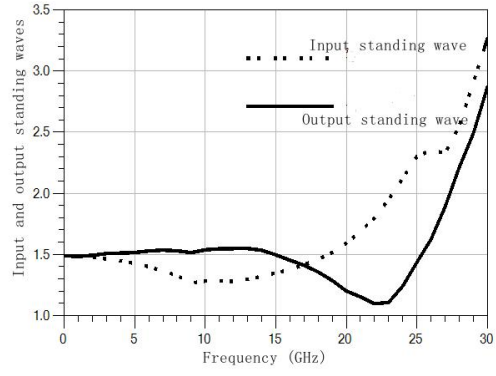


OUT3-ON

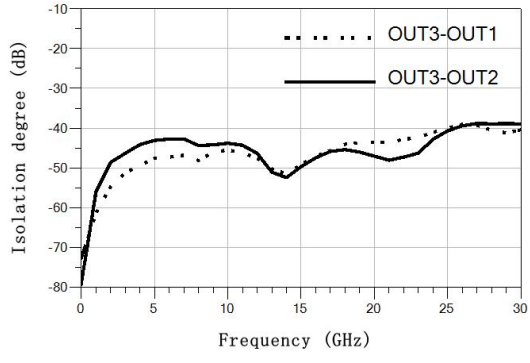
Insertion loss



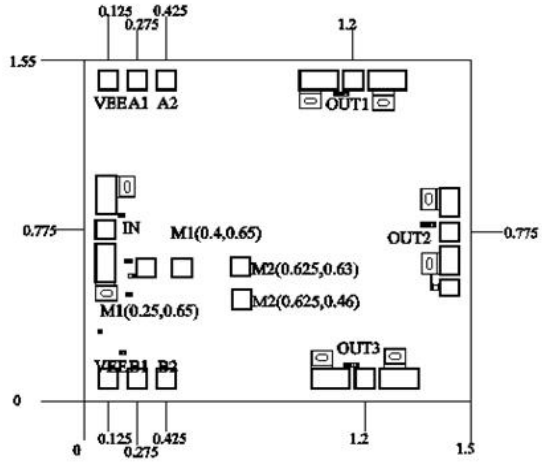
I/O standing wave



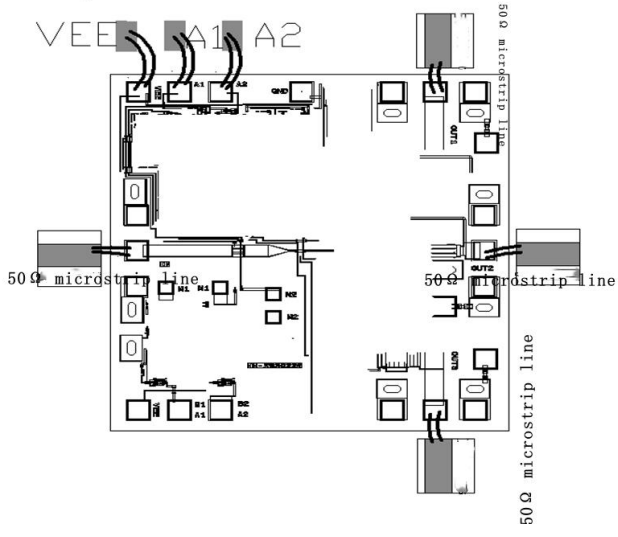
isolation



Size drawing：(unit mm)



Suggested assembly drawing：



Truth table:

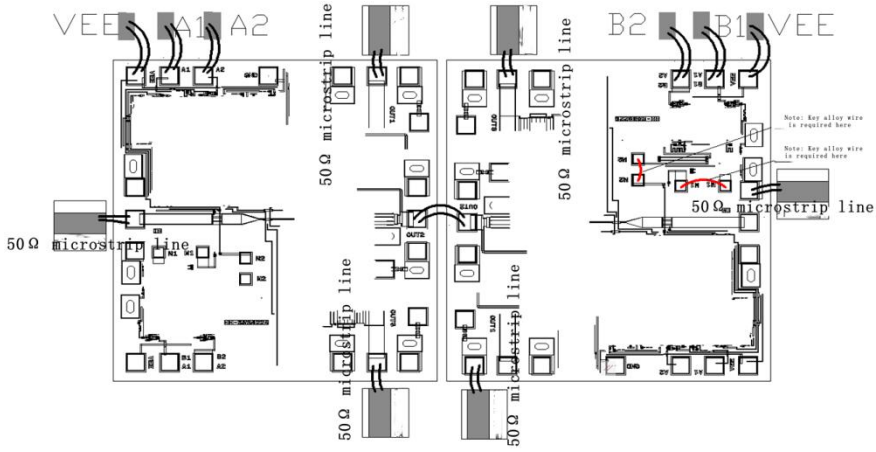
VEE	A1	A2	OUT1	OUT2	OUT3
-5	0	0	ON	OFF	OFF
-5	0	5	OFF	ON	OFF
-5	5	5	OFF	OFF	ON

Note:

1.VEE with -5V voltage;A1/A2 different power supply switching channel;

2. Add -5V voltage when mirroring;B1/B2 different power supply switching switch paths, which need to connect M1 to M1, M2 to M2 with gold wire (note: red connection line in the assembly drawing).

Recommended assembly drawing of cascade chip:



Truth table:

VEE	A1	A2	OUT1	OUT2	OUT3
-5	0	0	ON	OFF	OFF
-5	0	5	OFF	ON	OFF
-5	5	5	OFF	OFF	ON

Mirrored truth table:

VEE	B1	B2	OUT1	OUT2	OUT3
-5	5	5	ON	OFF	OFF
-5	5	0	OFF	ON	OFF
-5	0	0	OFF	OFF	ON

Instructions for use:

Storage: The chip must be placed in a container with electrostatic protection and stored in a nitrogen environment.

Cleaning treatment: The bare chip must be operated and used in a purified environment. It is forbidden to use liquid cleaning agent to clean the chip.

Electrostatic protection: Strictly comply with the ESD protection requirements to avoid electrostatic damage to the components.

General operation: Use vacuum chuck or precision pointed tweezers to pick up the chip.Avoid touching the surface of the chip with tools or fingers during handling.

Mounting operation: The chip can be installed using AuSn solder eutectic welding or conductive adhesive bonding process.The mounting surface must be clean and flat.

Bonding operation: Input and output with 2 (recommended diameter of 25um gold wire) bonding wire, bonding wire length less than 250um is optimal.It is recommended to use the smallest possible ultrasonic energy.Bonding begins at the pressure point on the chip and ends at the package (or substrate).