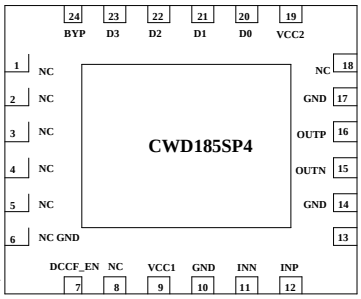
Performance Features

- Operating frequency: DC~8GHz
- Single sideband phase noise: -157dBc@100KHz N=2
- Output Power: 1dBm
- Power consumption: 157mA
- Package specification: QFN 4*4 24L

Typical Applications

- Cellular/3G Infrastructure

Functional Block Diagram



Overview

The CWD185SP4 is a low-noise continuously programmable crossover in a 4*4mm QFN 24L package, operating from DC to 8GHz, with phase noise below -The internal duty cycle correction circuit can be turned on via the DCCF_EN pin, and the output duty cycle is 33%~67% when the signal is turned on.

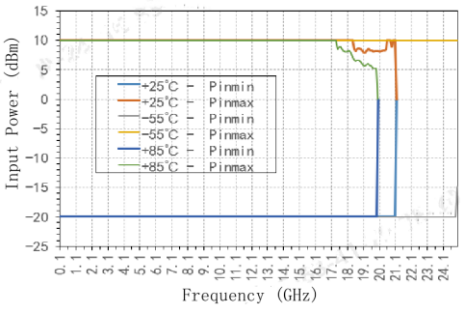
Under this function, the phase noise is optimized.

Electrical performance table (TA=+25℃, VCC1=VCC2=3~3.6)

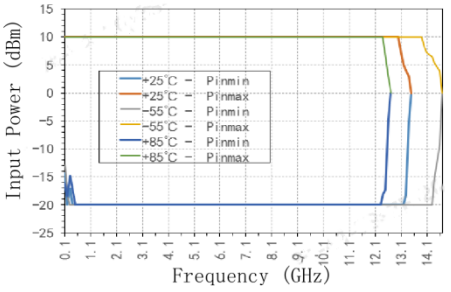
Parameter Name	Minimum value	Typical values	Maximum value	Unit	Test conditions
Input Frequency Range	0.2		8	GHz	Input Sine Wave
	DC		0.2	GHz	Input square wave with swing rate greater than 2V/ns
Input power range	-15		5	dBm	fin≥1GHz
Output power		0		dBm	DCCF_EN=1
Phase noise @1kHz		-150		dBc	fin=6G, Pin=0dBm, DIV2
Phase noise @10kHz		-155		dBc	
Phase noise @ 100kHz		-157		dBc	
Phase noise @ 1MHz		-157		dBc	
Phase noise @1kHz		-136		dBc	fin=6G, Pin=0dBm. DIV17 turns off duty cycle adjustment (DCCF_EN=0)
Phase noise @10kHz		-165		dBc	
Phase noise @ 100kHz		-164		dBc	
Phase noise @ 1MHz		-164		dBc	
Phase noise @1kHz		-130		dBc	fin=6G, Pin=0dBm. DIV17 turns on duty cycle adjustment (DCCF_EN=1)
Phase noise @10kHz		-161		dBc	
Phase noise @ 100kHz		-165		dBc	
Phase noise @ 1MHz		-167		dBc	
Power consumption current		157		mA	DIV17 Off Duty Cycle Adjustment
		176		mA	DIV17 turns on duty cycle adjustment

Test Curve

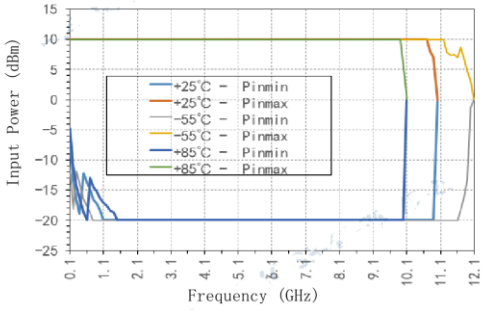
1-division RFOUT Crossover Sensitivity VS Frequency



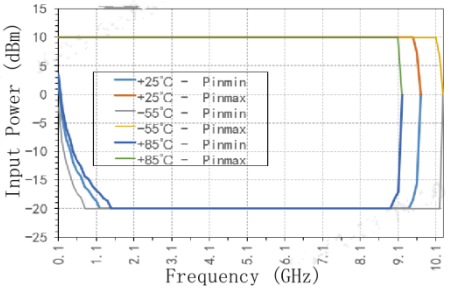
2-way RFOUT Crossover Sensitivity VS Frequency



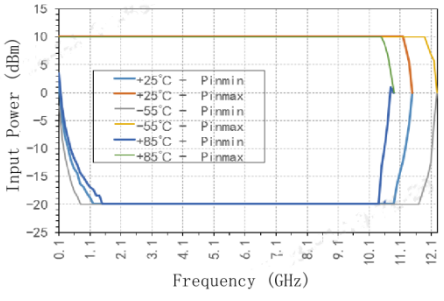
4-way RFOUT Crossover Sensitivity VS Frequency



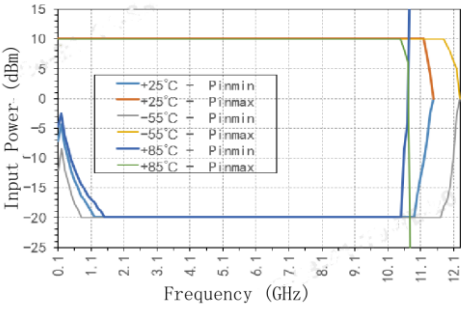
5-division RFOUT Crossover Sensitivity VS Frequency



13-division RFOUT Crossover Sensitivity VS Frequency

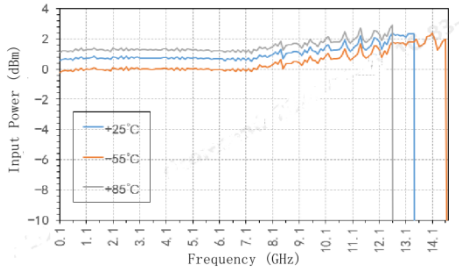


17-division RFOUT Crossover Sensitivity VS Frequency

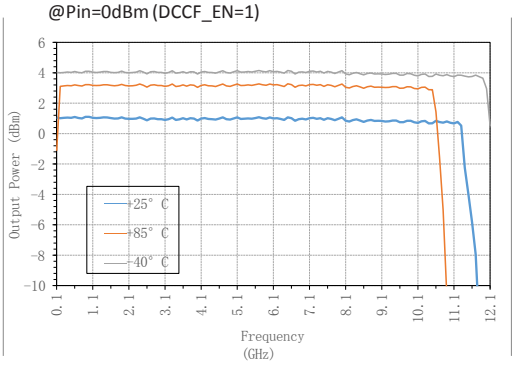


Test Curve

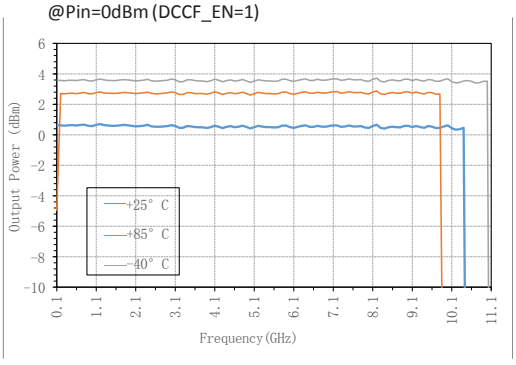
2-division Output Power VS Frequency
@Pin=0dBm (DCCF_EN=1)



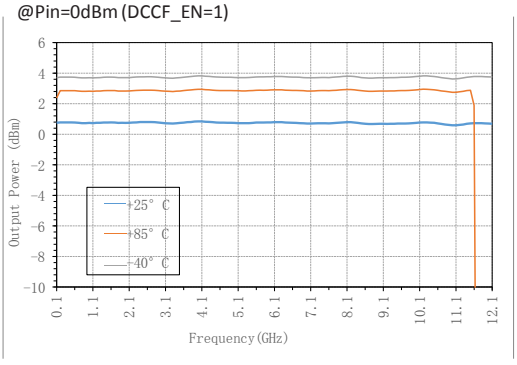
4-division Output Power VS Frequency
@Pin=0dBm (DCCF_EN=1)



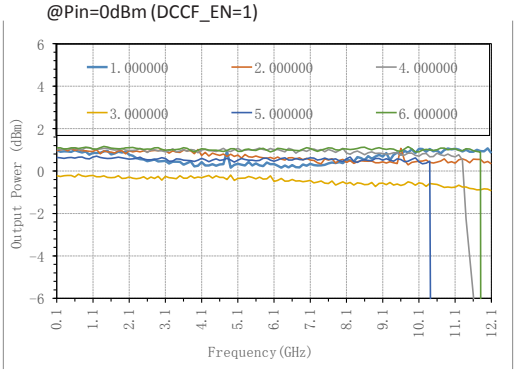
5-division Output Power VS Frequency
@Pin=0dBm (DCCF_EN=1)



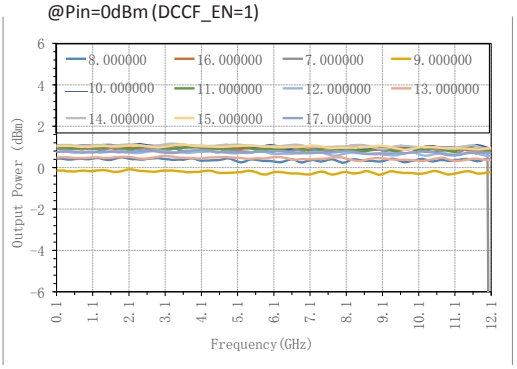
17-division RFOUT output power VS frequency
@Pin=0dBm (DCCF_EN=1)



N Division Output Power VS Frequency
@Pin=0dBm (DCCF_EN=1)



N Division Output Power VS Frequency
@Pin=0dBm (DCCF_EN=1)

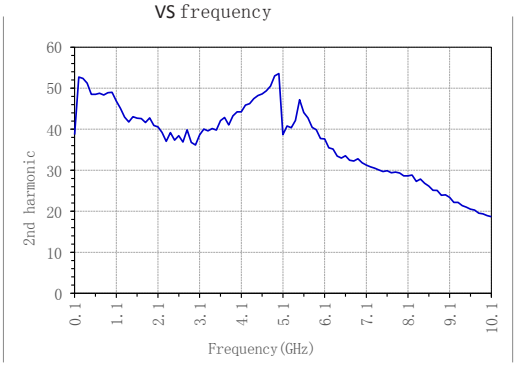


CWD

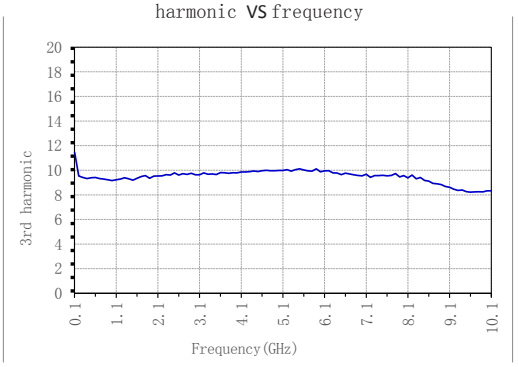
Programmable Frequency Divider

Test Curve

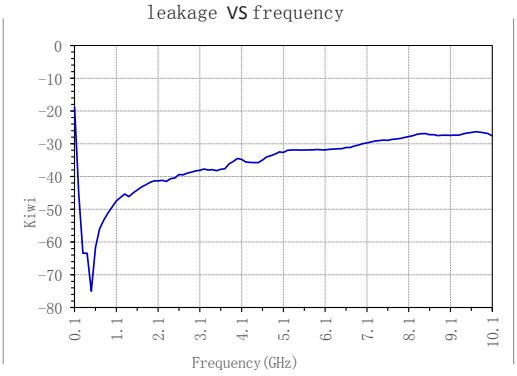
2-way 2nd harmonic VS frequency



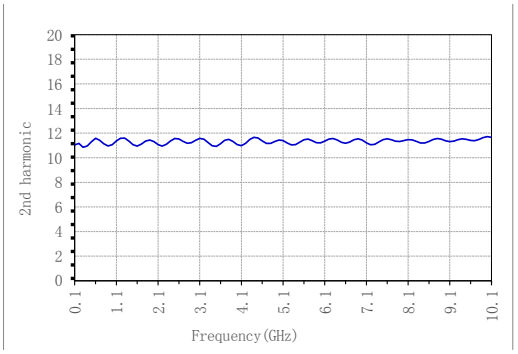
2nd division 3rd harmonic VS frequency



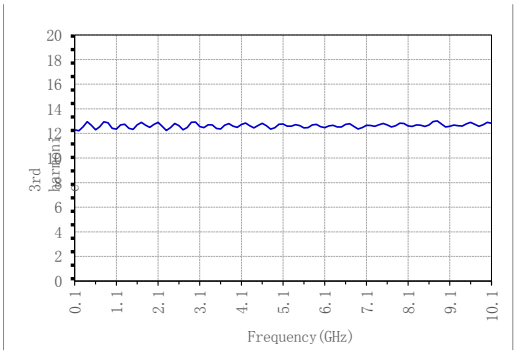
17-division Baseband leakage VS frequency



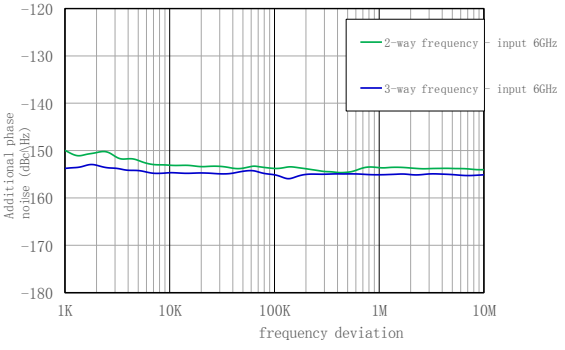
17 division 2nd harmonic VS frequency



17 division 3rd harmonic VS frequency



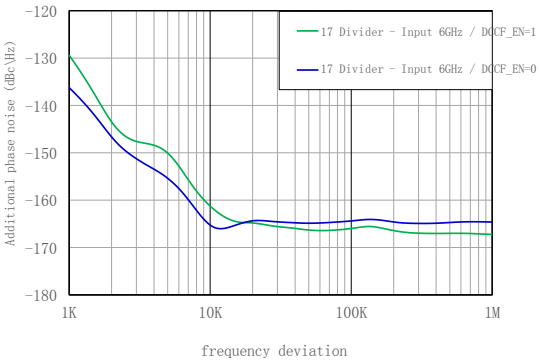
2&3 crossover frequency Phase noise



Chengdu Cuiwei Electronic Co. LTD
Address: No. 5, Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

Test Curve

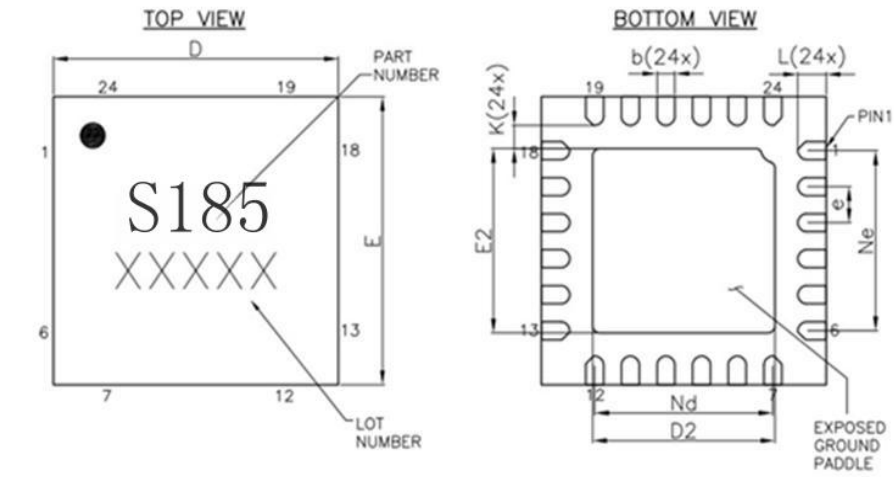
17 crossover frequency Phase noise



Absolute Maximum

Parameters	Scope
VCC1, VCC2	-0.3V~3.6V
IO Port	-0.3V~VCC+0.3V
Operating temperature	-40℃~85℃
Storage temperature	-65℃~150℃
ESD(HBM)	1000V

Chip Package Outline Diagram

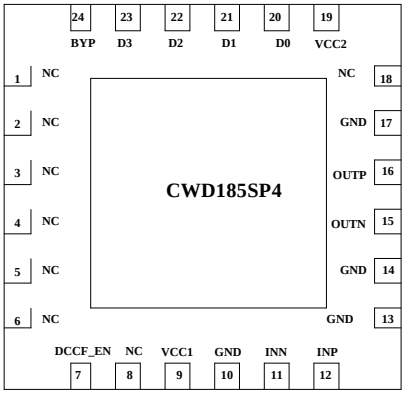


SP4 Dimension Table (unit:mm)

Symbol	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.20Ref	
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D2	2.41	2.56	2.66
e		0.50BSC	
Ne		2.50BSC	
Nd		2.50BSC	
E	3.90	4.00	4.10
E2	2.41	2.56	2.66
K	0.20	---	---
L	0.30	0.40	0.50
ccc		0.08	

Description.
1.Unit: mm
2.Lead frame material: copper alloy
3. Package surface warpage; ≤0.05m
4.All ground pins should be connected to PCB RF ground

Pad shape and description



PIN number	Name	Description
7	DCCF_EN	Logic input port, switch duty cycle shaping function, internal 80kΩ pull-up integrated 3.3V TTL level
9	VCC1	Crossover power port
10, 13, 14, 17	GND	Grounding port
11	INN	RF reverse input port
12	INP	RF isotropic input port
15	OUTN	Crossover reverse output port
16	OUTP	Crossover coaxial output port
19	VCC2	Output stage power port
20~23	D0~D3	Logic input port, controlling the crossover ratio. 3.3V TTL level
24	BYP	Logic input port, control bypass or not

Control instructions

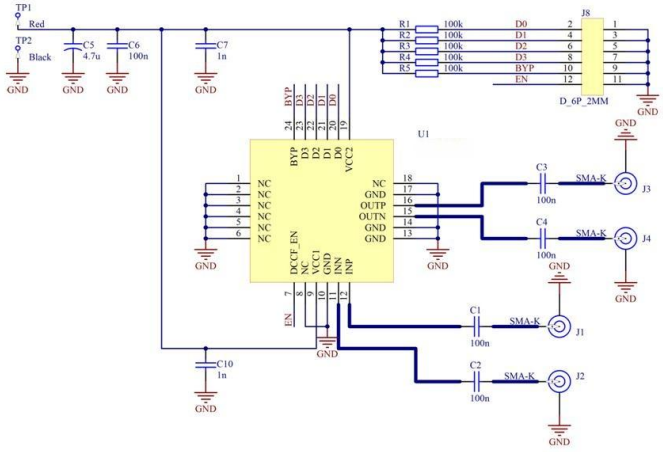
BYP	D3	D2	D1	D0	Crossover Number MOD
1	x	x	x	x	1
0	0	0	0	0	2
0	0	0	0	1	3
0	0	0	1	0	4
0	0	0	1	1	5
0	0	1	0	0	6
0	0	1	0	1	7
0	0	1	1	0	8
0	0	1	1	1	9
0	1	0	0	0	10
0	1	0	0	1	11
0	1	0	1	0	12
0	1	0	1	1	13
0	1	1	0	0	14
0	1	1	0	1	15
0	1	1	1	0	16
0	1	1	1	1	17

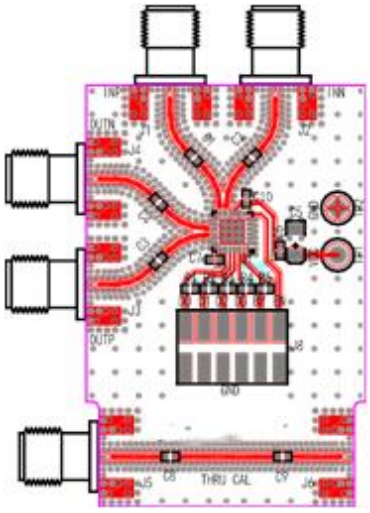
Duty cycle shaping function description:

The DCCF_EN pin is the duty cycle shaping control pin. When DCCF_EN is connected high or suspended, the internal duty cycle shaping function is enabled, and the function is effective when the number of dividers is greater than 4.

Chengdu Cuiwei Electronic Co. LTD
Address: No. 5, Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

Evaluation Board Circuit Diagram





Designator	Description
C1, C2, C3. C4	Multilayer Ceramic Capacitor 0402 100nF
C5	Tantalum capacitor 1206 4.7uF
C6	Multilayer Ceramic Capacitor 0402 100nF
C7, C10	Multilayer Ceramic Capacitor 0402 1nF
R1, R2, R3. R4, R5	Resistance 0402 100kΩ
J8	2.0mm DC pins
J1, J2, J3. J4	SMA-K PCB Connectors
TP1, TP2	DC test terminal
U1	CWD185SP4
J1, J2, J3, J4 Recommended for use with Nanjing Aowen D550B12E01-SMA-K connector type 023	
NC indicates that the port is not used or the device is not soldered. The outside of the chip NC port can be connected to GND.	