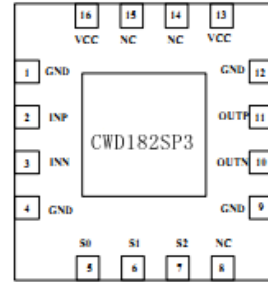


### Performance Features

- Operating frequency band: DC ~ 26GHz
- Single sideband phase noise: -156dBc@100KHz N=2
- Output Power: 1dBm
- Power consumption: 101mA
- Package size: QFN 3\*3 16 L

### Typical Applications Functional Block Diagram

- Cellular/3G Infrastructure



### Overview

The CWD182SP3 is a low-noise programmable crossover with N=1, 2, 4, 8, 16, 32, 64, 128, in a 3\*3mm QFN16 package, operating from DC to 26GHz, with phase noise below -156dBc@100kHz under typical operating conditions.

### Electrical performance table (TA=-40 °C ~ +85 °C , VCC = 3 ~ 3.6V)

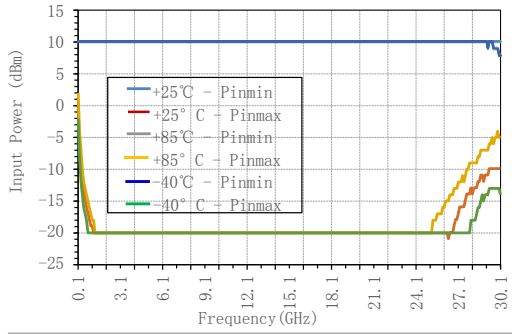
Parameter Name	Minimum value	Typical values	Maximum value	Unit	Test conditions
Input Frequency Range	0.1		26	GHz	Input Sine Wave
	DC		0.1	GHz	Input square wave with swing rate greater than 2V/ns
Input power range	-18		+8	dBm	fin=1~24G
	-10		+8	dBm	fin=24~26G
Output power		1		dBm	
Phase noise @1kHz		-150		dBc	fin=8G, Pin=0dBm, DIV2
Phase noise @10kHz		-155		dBc	
Phase noise @ 100kHz		-156		dBc	
Phase noise @ 1MHz		-157		dBc	
Phase noise @1kHz		-153		dBc	fin=8G, Pin=0dBm, DIV4
Phase noise @10kHz		-158		dBc	
Phase noise @ 100kHz		-159		dBc	
Phase noise @ 1MHz		-159		dBc	
Phase noise @1kHz		-146		dBc	fin=16G, Pin=0dBm, DIV2
Phase noise @10kHz		-149		dBc	
Phase noise @ 100kHz		-152		dBc	
Phase noise @ 1MHz		-152		dBc	
Phase noise @1kHz		-146		dBc	fin=16G, Pin=0dBm, DIV4
Phase noise @10kHz		-153		dBc	
Phase noise @ 100kHz		-154		dBc	
Phase noise @ 1MHz		-154		dBc	
Power consumption current		101		mA	DIV=8

### Test Curve

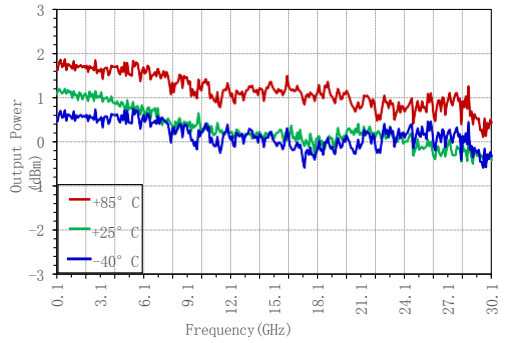
CWD

Fixed Frequency Divider

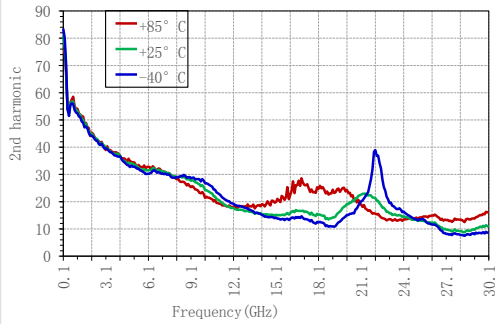
2-way RFOUT crossover sensitivity vs. frequency



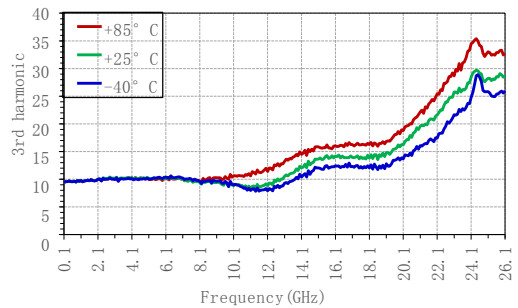
2-division RFOUT output power vs. frequency @Pin=0dBm



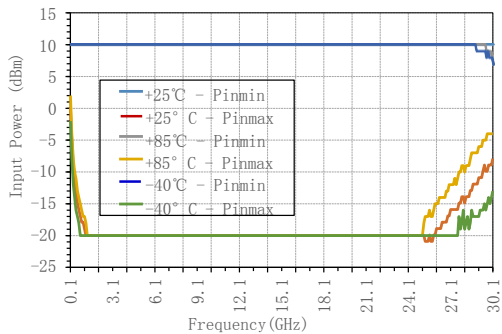
2-way 2nd harmonic vs. frequency



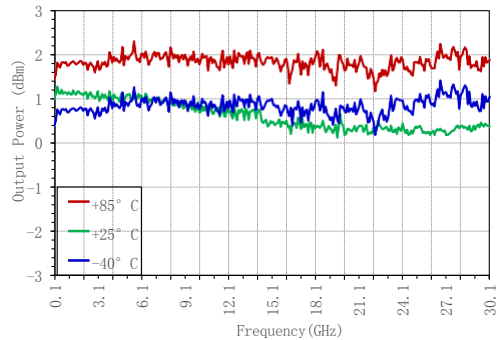
2nd division 3rd harmonic vs. frequency



4-division RFOUT crossover sensitivity vs. frequency

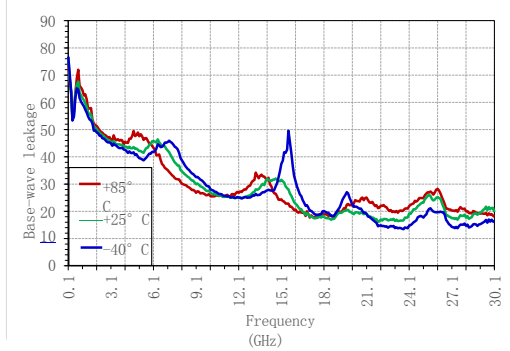


4-division RFOUT output power vs. frequency @Pin=0dBm

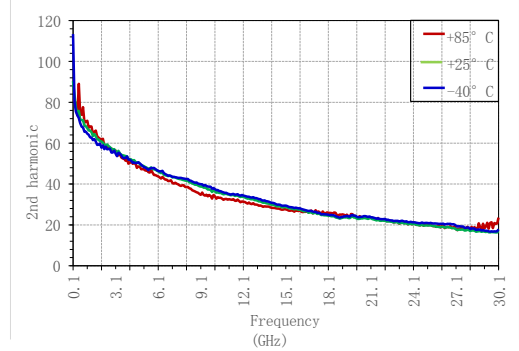


#### Test Curve

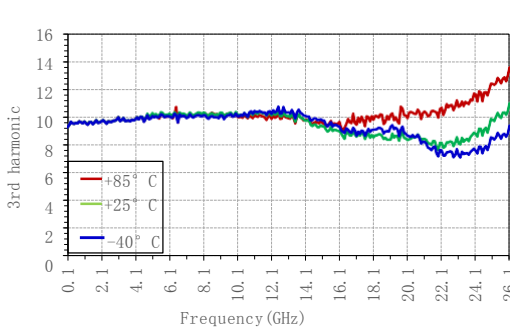
4-division Base-wave leakage vs. frequency



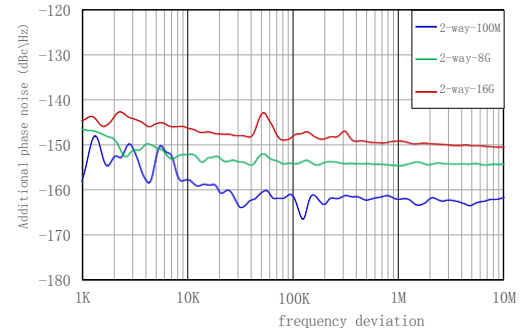
4-way 2nd harmonic vs. frequency



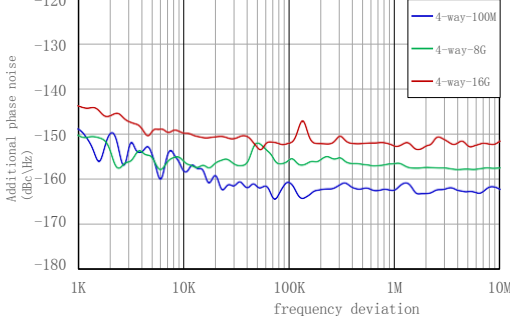
4 division 3rd harmonic vs frequency



2-way phase noise



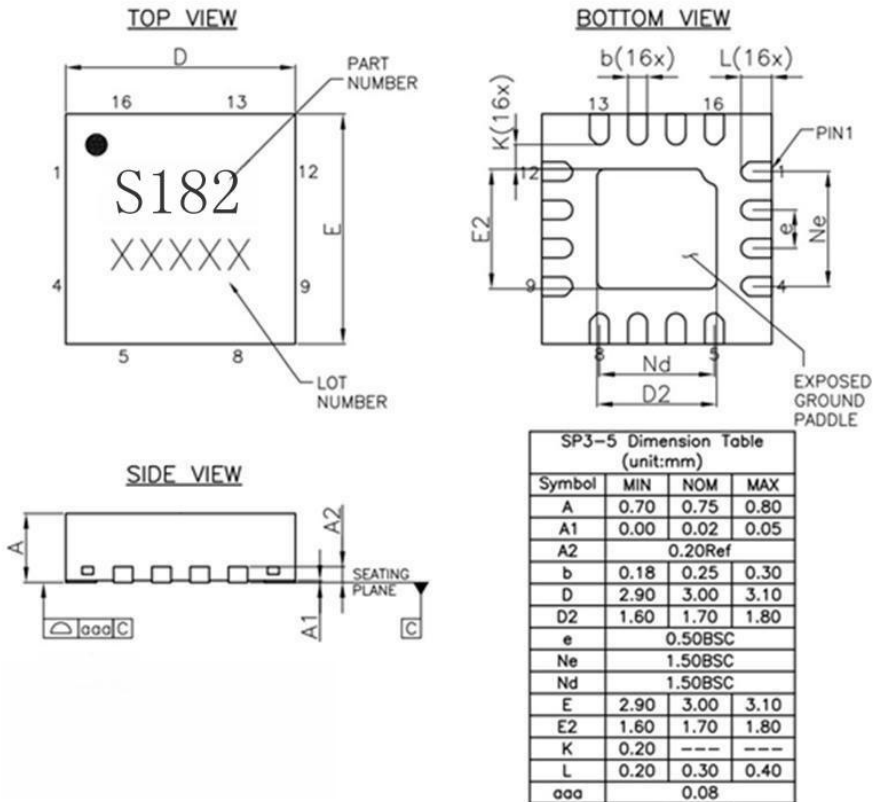
4-way phase noise



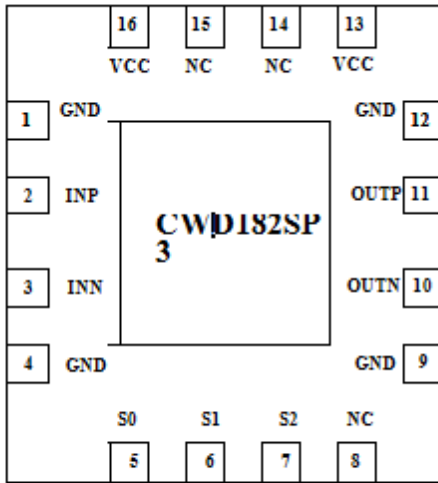
#### Absolute Maximum

Parameters	Scope
VCC	-0.3V~3.6V
I/O Port	-0.3V~VCC+0.3V
Operating temperature	-40°C~85°C
Storage temperature	-65°C~150°C
ESD (HBM)	1000V

#### Chip Package Outline Diagram



## Pad shape and description

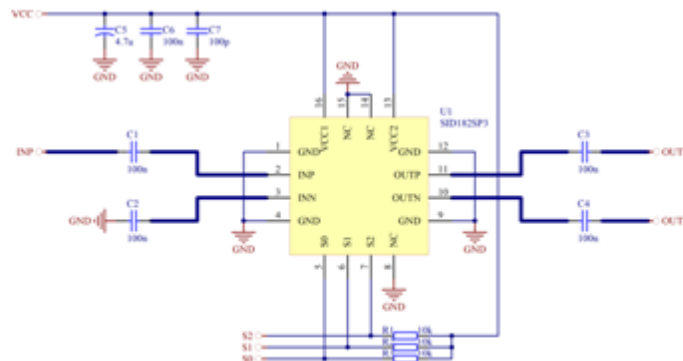


PIN number	Designation	Description
1, 4, 9, 12	GND	Grounding port
2	INP	RF isotropic input port
3	INN	RF reverse input port
5, 6, 7	S0-S2	Logic input, controlling the number of divisions, internally integrated under 80kΩ
10	OUTN	Crossover reverse output port
11	OUTP	Crossover isotropic output port
13, 16	VCC	Power port

## Control instructions

S2	S1	S0	分频数 MOD
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

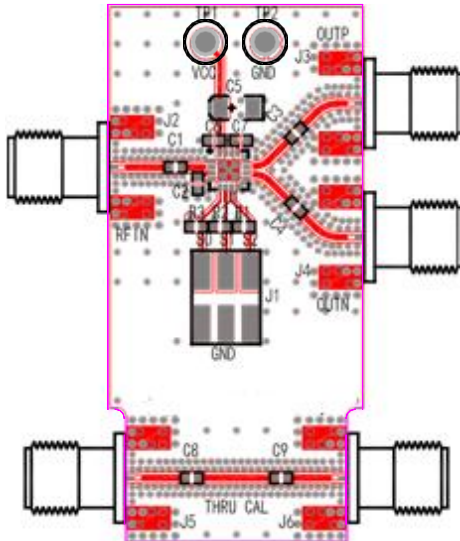
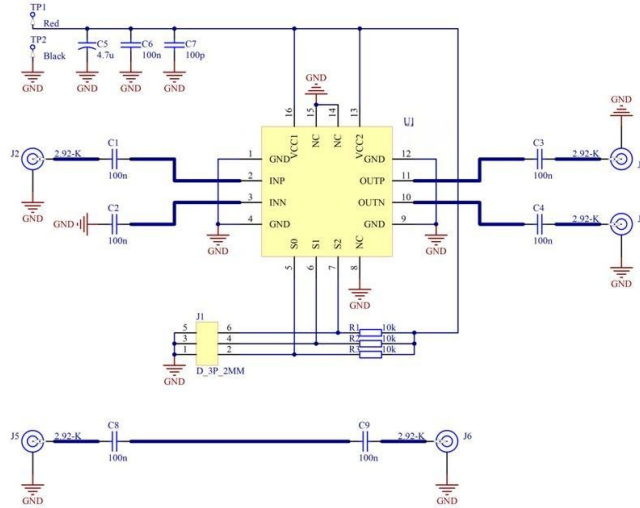
## Typical application diagram



#### Evaluation Board Circuit Diagram

CWD

Fixed Frequency Divider



Designator	Description
C1, C2, C3. C4, C6	Multilayer Ceramic Capacitor 0402 100nF
C5	Tantalum capacitor 1206 4.7uF
C7	Multilayer Ceramic Capacitor 0402 100pF
R1, R2, R3	Resistance 0402 10kΩ
J1	2.0mm DC pins
J2, J3, J4	2.92-K PCB Connectors
TP1, TP2	DC test terminal
U1	CWD182SP3
J2, J3, J4 Recommended for Nanjing Aowen D360B12E01-023	
2.92-K connectors	
NC indicates that the port is not used or the device is not soldered. The outside of the chip NC port can be connected to GND.	