

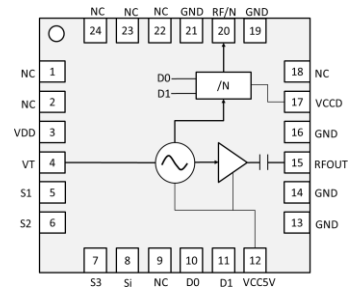
Performance Features

- Operating frequency band: 10 GHz to 20 GHz
- Low power consumption: 162mA (VCC5V side)
- Output power: 7 dBm (RFOUT side)
- Phase noise: -101dBc/Hz@100kHz
- Package size: 24-pin QFN, 4mmx4mm

Typical Applications

- Point-to-Point Communication
- Satellite Communications
- Test measurements
- Instrumentation

Functional Block Diagram



Overview

The CWV100SP4 is a low-noise, low-power voltage controlled oscillator, a multi-band broadband VCO with integrated crossover function and gapless coverage of 2:1 output frequency. It has independent /2, /4, /8, and /16 programmable crossover output ports.

The CWV100SP4 is a 24-pin 4mmx4mm surface mount leadless plastic package. The pin pads are coated with NiPdAuAg.

Electrical performance table (TA=+25°C,VDD=VCCD=3.3V,VCC5V=5V)

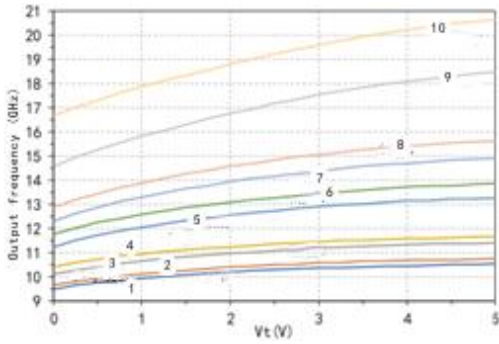
Parameter Name	Port Name	Minimum value	Typical values	Maximum value	Unit
RF Frequency Range	RFOUT	10~20			GHz
RF/N Frequency Range	RF/N	0.625~10			GHz
RF side output power	RFOUT	0	7	11	dBm
Programmable crossover terminal output power	RF/N (N=2)	-5	-1.5	0.5	dBm
Programmable crossover terminal output power	RF/N (N=4, 8, 16)	-3	-1	0.5	dBm
RF port single sideband phase noise @ 100kHz frequency bias			-101		dBc/Hz
Tuning voltage	VT	0		5	V
Bias voltage	VCC5V		5		V
	VDD, VCCD		3.3		V
Bias current	Icc5V		162		mA
	Iccd (N=2)		19		mA
	Iccd (N=4)		25		mA
	Iccd (N=8)		28		mA
	Iccd (N=16)		30		mA
Leakage current at the tuning end (Vt=+5V)			10		μA
RF port return loss			8		dB
Push frequency factor			25		MHz/V
Switching time between frequency bands			50		ns
RF port harmonics, sub-harmonic suppression	1/2		36		dBc
	3/2		30		dBc
	2nd		22		dBc
	3rd		33		dBc

Test Curve

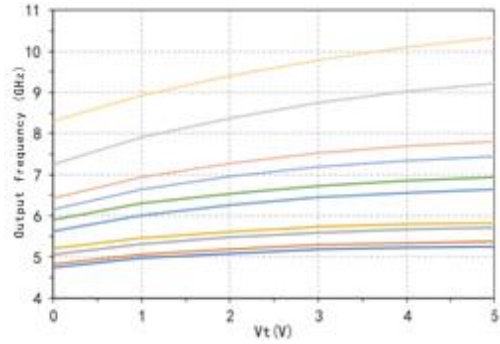
CWV

Voltage Controlled Oscillator Series

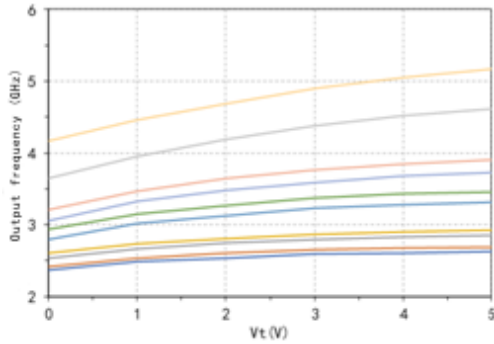
RFOUT output frequency VS Vt



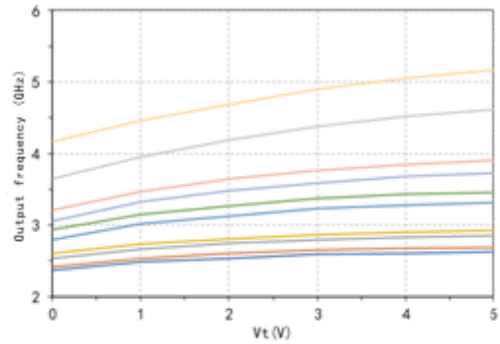
RF/N output frequency VS Vt (N=2)



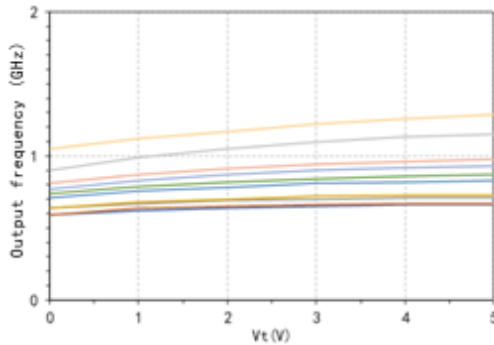
RF/N output frequency VS Vt (N=4)



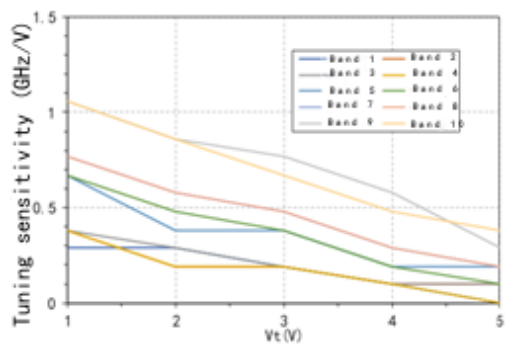
RF/N output frequency VS Vt (N=8)



RF/N output frequency VS Vt (N=16)

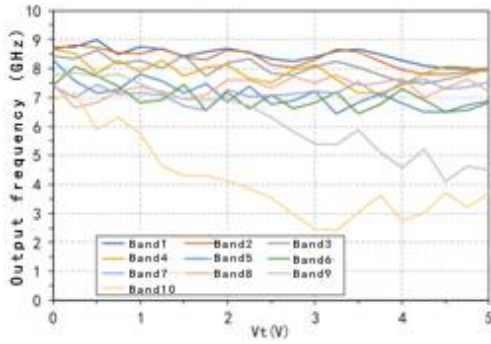


RFOUT tuning sensitivity VS Vt

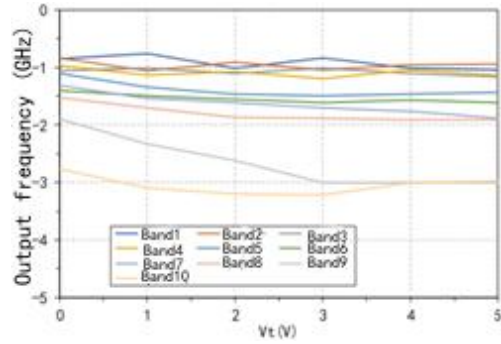


Test Curve

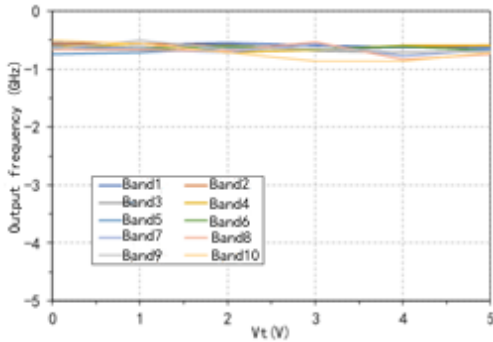
RFOUT output power VS Vt



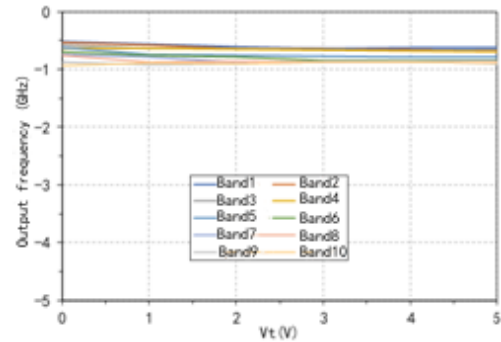
RF/N output power VS Vt (N=2)



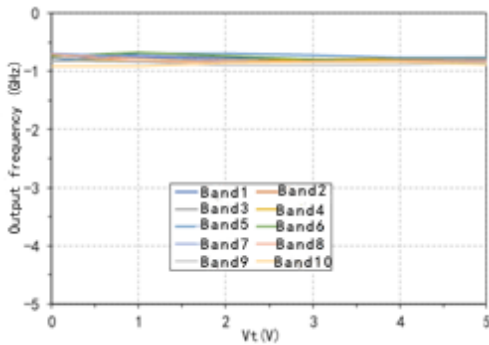
RF/N output power VS Vt (N=4)



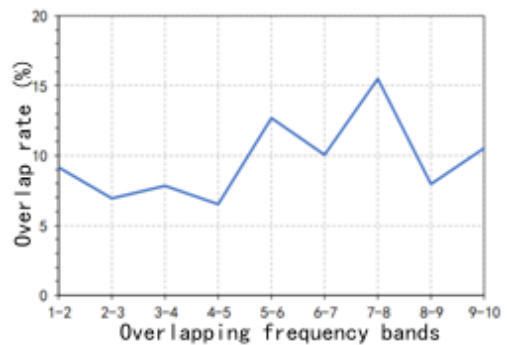
RF/N output power VS Vt (N=8)



RF/N output power VS Vt (N=16)



RFOUT band overlap percentage VS overlapping bands

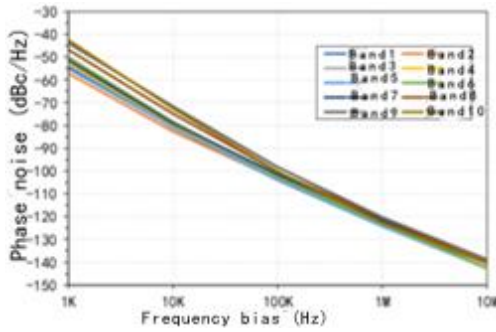


Test Curve

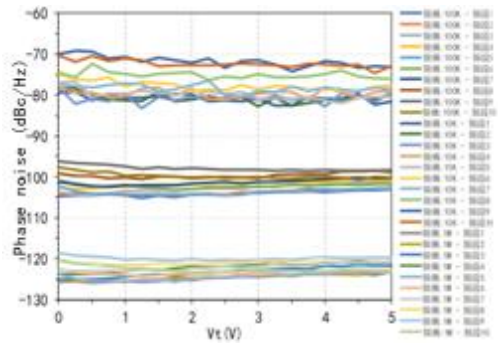
CWV

Voltage Controlled Oscillator Series

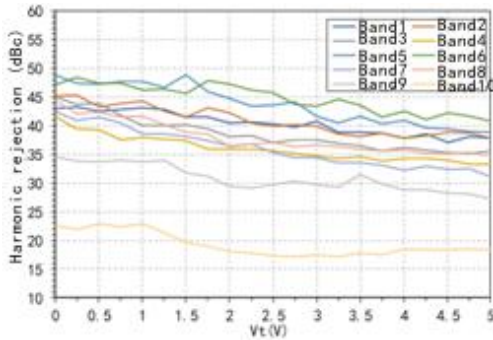
RFOUT phase noise vs. frequency bias @ Vt=3V



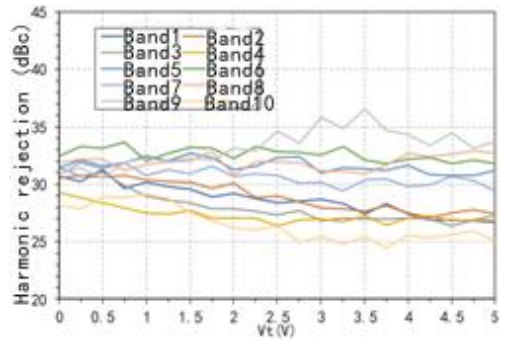
RFOUT phase noise VS Vt



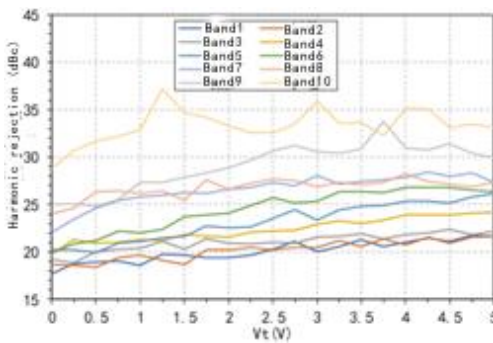
1st/2nd harmonic suppression VS Vt



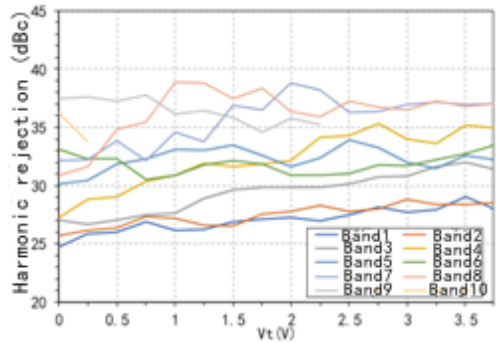
3rd/2nd harmonic suppression VS Vt



2nd harmonic suppression VS Vt



3rd harmonic suppression VS Vt



Extreme operating parameters

Bias voltage	5.5V (VCC5V)
	3.6V (VDD, VCCD)
Tuning voltage	0V to 5.5V
Storage temperature range	-65°C~+150°C
Operating temperature range	-40°C~+85°C
Electrostatic protection level (HBM)	Class 1B

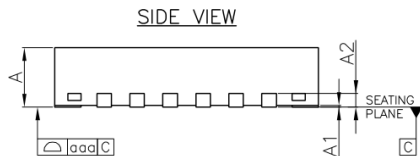
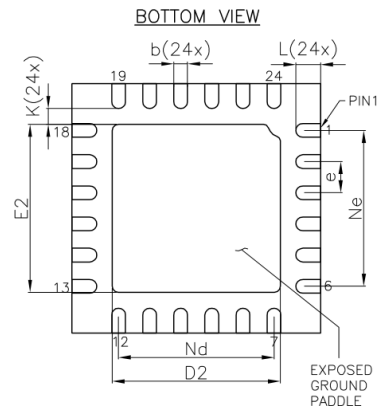
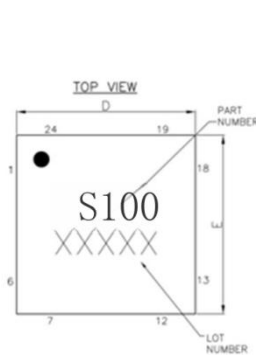
Package Information

Model	Packaging Materials	Solder plate plating	MSL level [1]	Package identification [2]	Environmental requirements
CWV100SP4	Green resin compounds	NiPdAuAg	MSL 3	S100 XXXXX	RoHS compliant

[1] Maximum reflow temperature 260° C

[2] XXXXX is the lot number

Dimension



Symbol	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.20Ref		
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D2	2.55	2.70	2.80
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.55	2.70	2.80
K	0.20	---	---
L	0.30	0.40	0.50
aaa	0.08		

Description:

- Unit: mm
- Lead frame material: copper alloy
- Package surface warpage: not more than 0.05mm
- All ground pins should be connected to PCB RF ground

Pin Definition

Pin Number	Function Symbols	Function Description	Pin Number	Function Symbols	Function Description
1	NC	Vacant	13	GND	RF Ground
2	NC	Vacant	14	GND	RF Ground
3	VDD	DC Bias	15	RFOUT	RF Output
4	VT	Tuning voltage	16	GND	RF Ground
5	S1	Logic Control	17	VCCD	DC Bias
6	S2	Logic Control	18	NC	Vacant
7	S3	Logic Control	19	GND	RF Ground
8	Si	Logic Control	20	RF/N	RF Output
9	NC	Vacant	21	GND	RF Ground
10	D0	Logic Control	22	NC	Vacant
11	D1	Logic Control	23	NC	Vacant
12	VCC5V	DC Bias	24	NC	Vacant

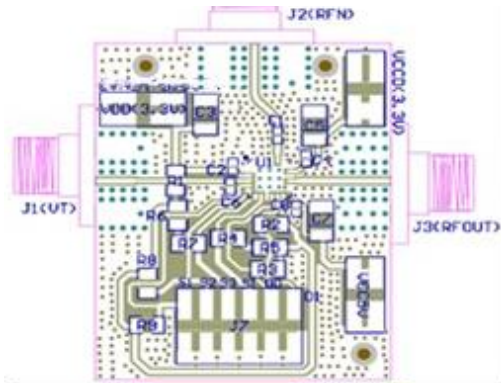
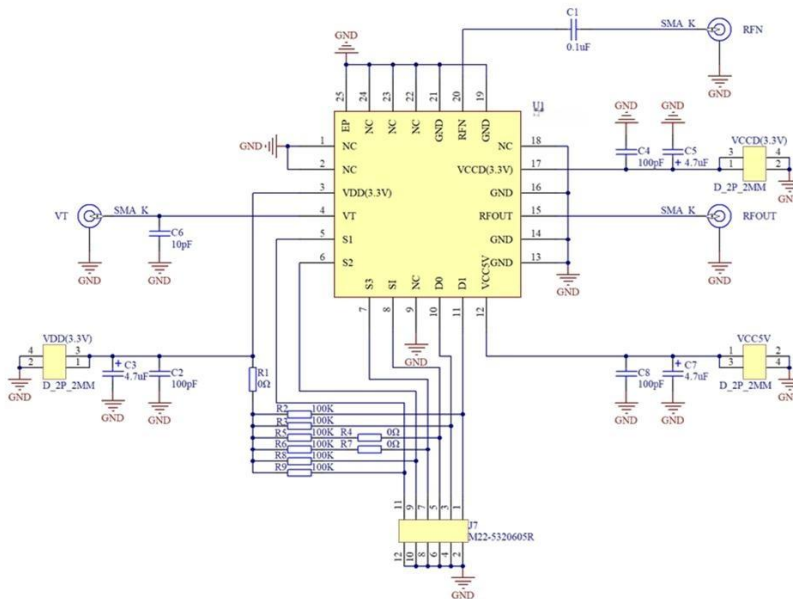
Logic control parameters

Programmable Frequency Divider Output Truth Table		
D1	D0	Frequency division ratio (N)
0	0	2
0	1	4
1	0	8
1	1	16

Logical State	d0, d1, s1, s2, s3, si
0	0V~0.3V
1	3V~3.3V

Recommended Logic Control States				Output Frequency Band
S1	S2	S3	Si	
0	0	0	1	Band 1
1	0	0	1	Band 2
0	1	0	1	Band 3
1	0	0	0	Band 4
0	0	1	1	Band 5
1	0	1	1	Band 6
0	0	1	0	Band 7
1	0	1	0	Band 8
0	1	1	0	Band 9
1	1	1	0	Band 10

Other states are not evaluated



Circuit board material: Rogers 4350B

The circuit board of the device application should be designed according to the RF circuit design method, the signal line should be designed according to the 50 ohm impedance, and the ground pin of the package shell should be grounded nearby (similar to the figure), and there should be enough grounding holes to connect the top and bottom ground layers.

Designator	Description
C1	Multilayer ceramic capacitor 0402 0.1uF
C2, C4, C8	Multilayer ceramic capacitor 0402 100pF
C3, C5, C7	Tantalum capacitor 1206 4.7uF
C6	Multilayer ceramic capacitor 0402 10pF
R1, R4, R7	Resistor 0805 0Ω
R2, R3, R5, R6, R8, R9	Resistor 0805 100K
J1, J2, J3	SMA PCB connector
VCC5V, VCCD(3.3V), VDD(3.3V)	2 mm DC pins
J7	2 mm DC pins
U1	CWV100SP4
J1, J2, J3 are recommended to use Nanjing Aowen D550B12E01-048 type SMA connector	