

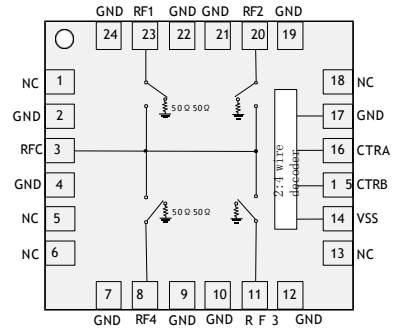
Performance Features

- Operating frequency band: DC ~ 20GHz
- Low insertion loss: 2dB@DC~12GHz typical
3.2dB@12~20GHz Typical
- High isolation: 50dB@DC~10GHz
55dB@10GHz~20GHz
- Package size: 24-pin QFN,
4mmx4mm

Typical Applications

- Base station communication
- Wireless Infrastructure
- Automotive Electronics
- Instrumentation

Functional Block Diagram



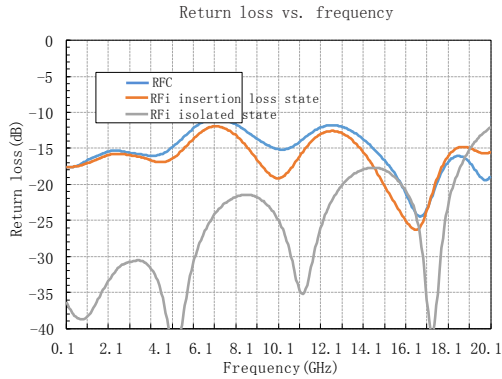
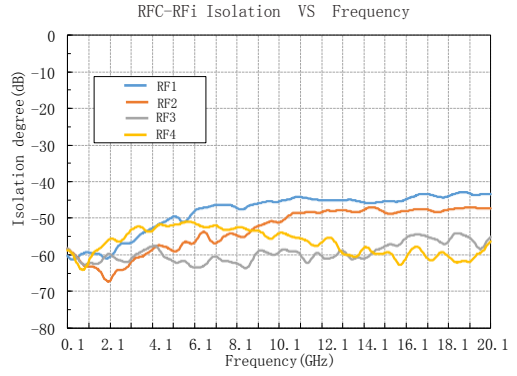
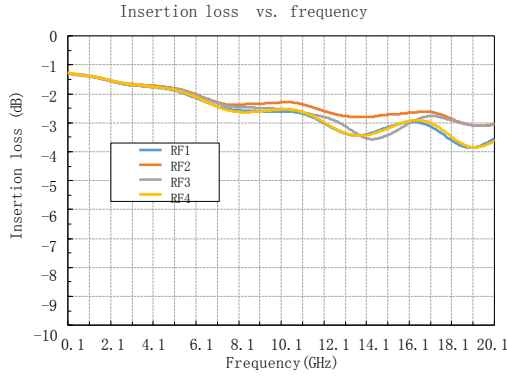
Overview

The CWS037SP4 is a highly isolated, low insertion loss, high linearity, absorptive single-blade, four-throw switch. The CWS037SP4 type switch is available in a 24-pin 4mmx4mm surface mount leadless plastic package. The pin pads are plated with Sn.

Electrical performance table (TA=+25°C, VSS=-5V)

Parameter Name	Test conditions	Minimum value	Typical values	Maximum value	Unit
RF Frequency Range		DC~20			GHz
insert loss	DC~12GHz		2		dB
	12GHz~20GHz		3.2		dB
Isolation	DC~10GHz		55		dB
	10GHz~20GHz (RF1、RF2)		47		dB
	10GHz~20GHz (RF3、RF4)		50		dB
Return loss	open state		12		dB
	Off-state		17		dB
Bias Voltage (VSS)		-5.2		-4.8	V
Bias current (ISS)				2	mA
Input 0.1dB compression point power (PO.1dB)			TBD		dBm
Input 1dB compression point power (P1dB)			22.6		dBm
Input third-order intercept point of intersection (IP3)			TBD		dBm
Rise and fall time	10% to 90% RF output		60		ns
Switching time	50% Vctl to 10%/90% RF output		130		ns
Recommended input power	Straight through state		21		dBm
	Isolated state		21		dBm

Test Curve

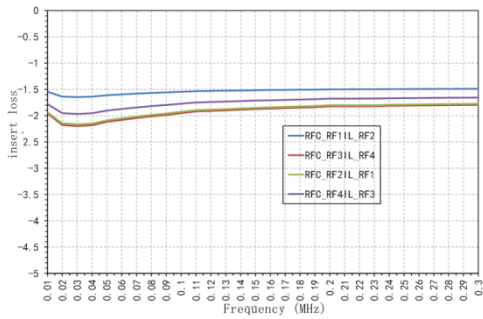


CWS

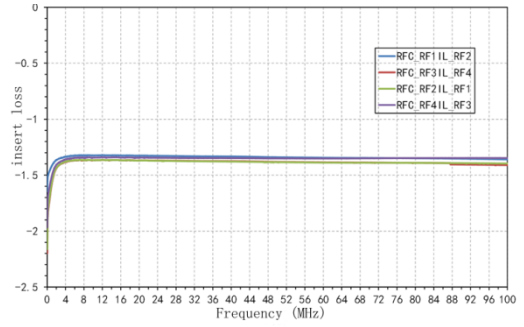
Switch regulator series

Test Curve

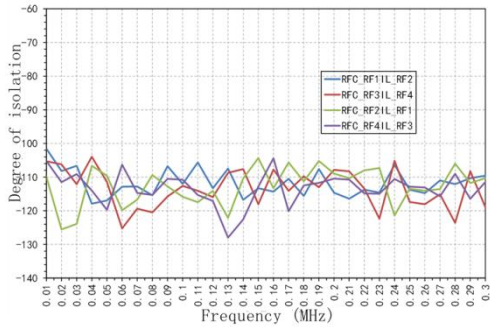
Insertion loss vs. frequency (@10K-300K)



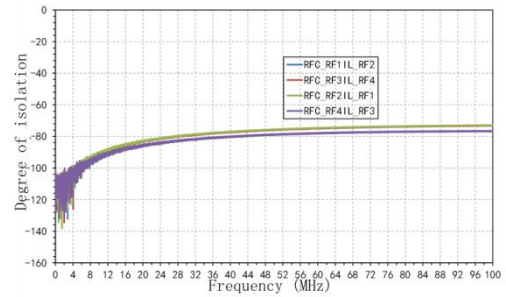
Insertion loss VS frequency (@10K-100M)



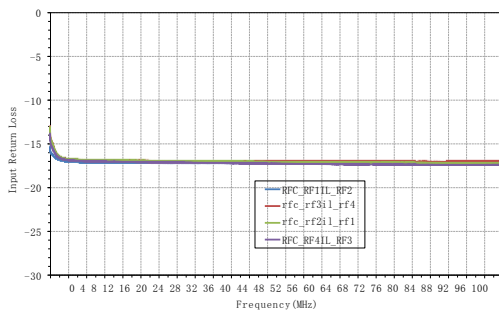
Isolation VS Frequency (@10K-300K)



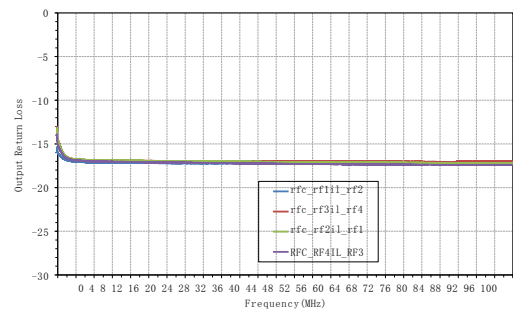
Isolation VS Frequency (@10K-100M)



Input Return Loss VS Frequency (@10K-100M)



Output Return Loss VS Frequency (@10K-100M)



Working parameters

Bias voltage VSS	-4.8V to -5.2V
Control voltage V_{CTRA} 、 V_{CTRB}	0V~0.8V (Low) 3V to 5V (High)
Operating temperature	-40°C~+85°C

Absolute maximum rating

Bias voltage VSS	-6.5V
Control voltage V_{CTRA} 、 V_{CTRB}	-VSS-0.5V
Input power (straight-through state)	+25dBm
Input power (isolated state)	+25dBm
Storage temperature	-65°C~+150°C

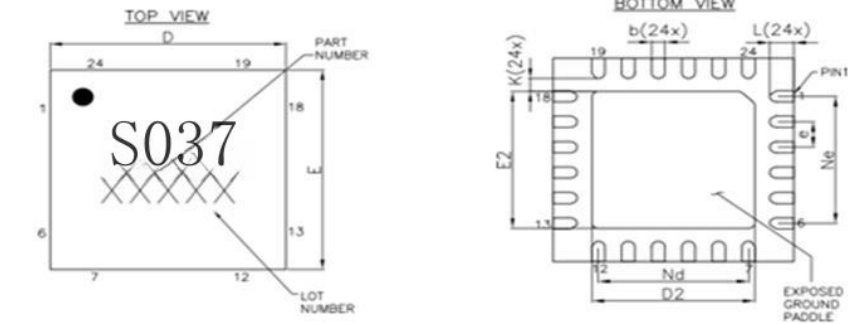
Package Information

Model	Packaging Materials	Solder plate plating	MSL level ⁽¹⁾	Package identification ⁽²⁾	Environmental requirements
CWS037SP4	Green resin compounds	Sn	MSL 3	S037 XXXXX	RoHS compliant

⁽¹⁾ Maximum reflow temperature 260° C

⁽²⁾ XXXXX is the lot number

Dimension



Symbol	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	---	0.05
A2	0.20Ref		
b	0.20	0.25	0.30
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
K	0.20	---	---
L	0.30	0.40	0.50
aaa	0.08		

Description:

1. Unit: mm
2. Lead frame material: copper alloy
3. Package surface warpage: not more than 0.05mm
4. All ground pins please connect PCB RF ground

Pin Definition

Pin Number	Function Symbols	Function Description	Pin Number	Function Symbols	Function Description
1	NC	Vacant	13	NC	Vacant
2	GND	RF Ground	14	VSS	Power supply
3	RFC	RF Common Side	15	CTRLB	Console B
4	GND	RF Ground	16	CTRLA	Console A
5	NC	Vacant	17	GND	RF Ground
6	NC	Vacant	18	NC	Vacant
7	GND	RF Ground	19	GND	RF Ground
8	RF4	RF 4-Port	20	RF2	RF 2 ports
9	GND	RF Ground	21	GND	RF Ground
10	GND	RF Ground	22	GND	RF Ground
11	RF3	RF 3-Port	23	RF1	RF 1 port
12	GND	RF Ground	24	GND	RF Ground

All NC pins are recommended to be connected to RF ground when in use

Truth Table

Control and bias inputs			Signaling pathway status
Bias Voltage (VSS)	Control A port	Control B port	
-5V	Low	Low	RFC to RF1
-5V	High	Low	RFC to RF2
-5V	Low	High	RFC to RF3
-5V	High	High	RFC to RF4

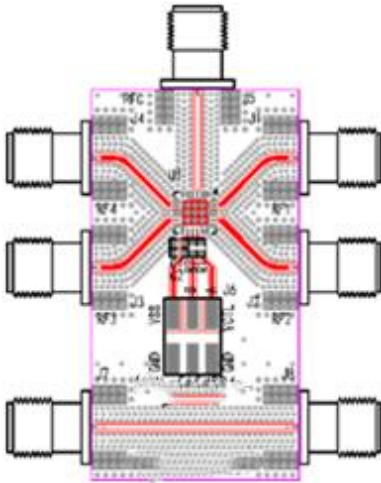
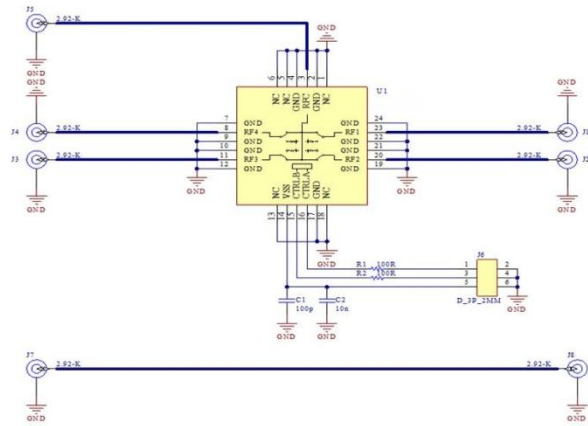
Working Principle

1. This switch requires a supply voltage to be applied to the VSS pin. It is recommended to bypass the capacitor on the power line to minimize RF coupling.
2. A 2:4 compiler is integrated inside this switch and the four RF paths are selected by two digital control voltages applied to the A and B control inputs. It is recommended to install a small bypass capacitor on these digital signal lines to improve the isolation of the RF signals.
3. The RF common port (RFC) and the RF output ports (RF1, RF2, RF3, RF4) are internally matched with 50Ω , so no external matching is required. The RF pins are direct-coupled, and the RF terminals need to be peripherally equipped with isolation capacitors. The design is bi-directional and the RF input signal can be applied to either the RFC port or the RF1 to RF4 port. The inputs and outputs are interchangeable.
4. Depending on the logic levels applied to the control input pins A and B, one RF output port (e.g., RF1) is set to open mode, which provides an insertion loss path from the input to the output. The other RF output ports (e.g., RF2, RF3, and RF4) are then set to the off mode, through which the output is isolated from the input. When the RF output ports (RF1, RF2, RF3, and RF4) are in isolated mode, they are internally terminated to 50Ω so that they can absorb the applied RF signal.

Recommended power supply sequence

1. GND is energized.
2. VSS is energized.
3. Turn on the digital control inputs. The relative order of the digital control inputs is not important. Powering on the digital control inputs before the VSS power supply may inadvertently cause bias and damage the ESD protection structure.
4. Turn on the RF input.

Evaluation Boards



Circuit board material: Rogers 4350B

The circuit board of the device application should be designed in accordance with the RF circuit design method, the signal line is designed according to 50Ω impedance, while the grounding pin of the package shell is grounded nearby (similar to the figure), connecting the top and bottom ground should have enough grounding holes.

Designator	Description
C1	100pF Ceramic Capacitor 0402
C2	10nF Ceramic Capacitor 0402
J1, J2, J3, J4, J5, J7, J8	2.92-K connector
J6	D_3P_2MM DC pin
R1, R2	100Ω 0402
U1	CWS037SP4
J1, J2, J3, J4, J5, J7, J8 Recommended for use with Nanjing Aowen D360B12E01-023 connector	