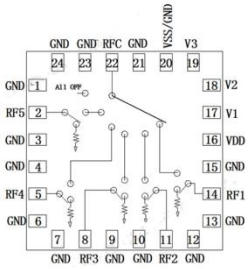
## Performance Features

- Operating frequency band: DC ~ 8GHz
- Low insertion loss: 1.3dB@9KHz～900MHz
  1.7dB@900MHz～2.6GHz
  2.3dB@2.6GHz～8GHz
- High isolation: -71dB@9KHz~900MHz
  -59dB@900MHz～2.6GHz
  -53dB@2.6GHz～8GHz
- Package size: 24-pin QFN, 4mmx4mm

## Typical Applications

- Base station communication
- Wireless Infrastructure
- Automotive Electronics
- Instrumentation

## Functional Block Diagram




## Overview

The CWS128SP4 is a highly reliable, low insertion loss, RF port matched to 50Ω single blade five-throw absorptive RF switch. It can be used in wireless and other RF systems. In addition to providing low insertion loss, the CWS128SP4 has high linearity and isolation, and its RF port is matched to 50

## Electrical performance table (TA=+25℃,VDD=3VVTRL=3.3V)

| Parameter Name | Test conditions | Minimum value | Typical values | Maximum value | Unit |
|---|---|---|---|---|---|
| RF Frequency Range | | DC ~ 8 | | | GHz |
| insert loss | 9KHz～900MHz | | 1.3 | | dB |
| | 900MHz～2.6GHz | | 1.7 | | dB |
| | 2.6GHz～8GHz | | 2.3 | | dB |
| Isolation | 9KHz～900MHz | | -71 | | dB |
| | 900MHz～2.6GHz | | -59 | | dB |
| | 2.6GHz～8GHz | | -53 | | dB |
| Return loss | Input Return Loss | | -12 | | dB |
| | Output Return Loss | | -12 | | dB |
| Bias Voltage (VDD) | | 3.0 | 5.0 | | V |
| Bias Current (IDD) | | | 1.0 | | mA |
| Input 1dB compression point power (P1dB) | | 31.0 | | | dBm |
| Input third-order intercept point of intersection (IP3) | DC～6GHz | | 48.0 | | dBm |
| Rise and fall time | 10% to 90% RF output | | | 45 | ns |
| Switching time | 50% Vctl to 10%/90% RF output | | | 145 | ns |
| Recommended input power | Insertion loss state | | | 28 | dBm |
| | Isolated state | | | 28 | dBm |

Note: The lowest frequency of the test instrument is only up to 10K, so only the test data above 10KHz is displayed.



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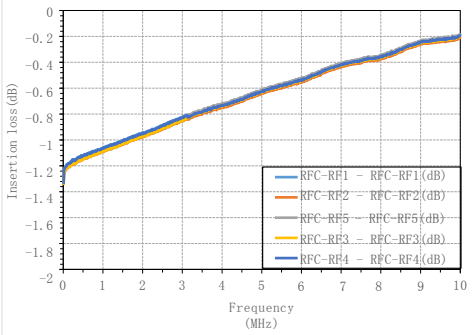
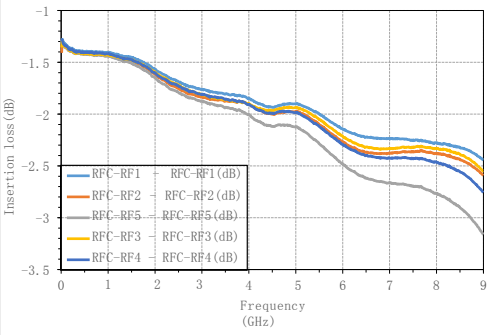
## Test Curve

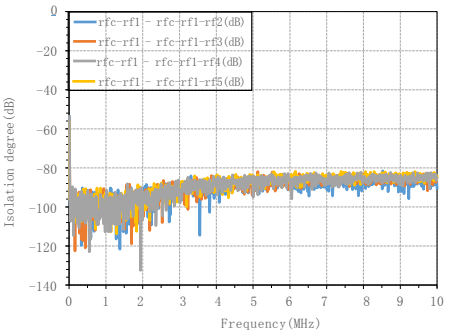
Insertion loss vs. frequency (10K-10M)



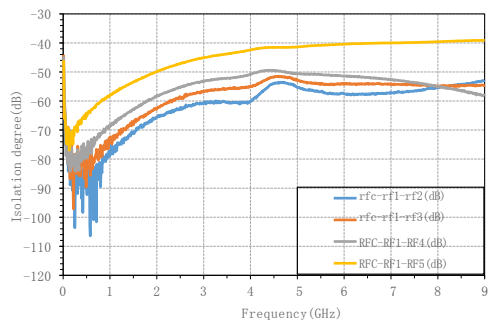

Insertion loss vs. frequency (10M-9G)



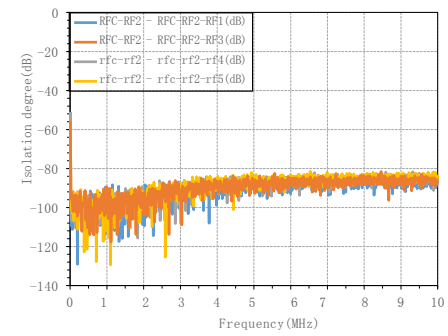

Isolation vs. frequency (10K-10M RF1: ON)



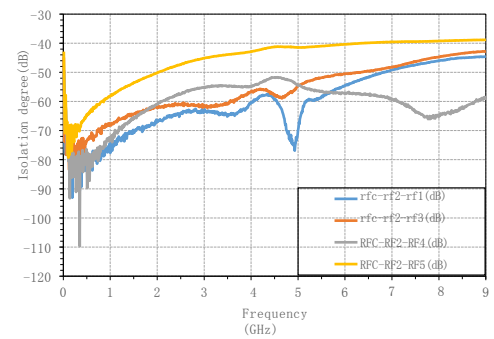

Isolation vs. frequency (10M-9G RF1: ON)




Isolation vs. frequency (10K-10M RF2: ON)




Isolation vs. frequency (10M-9G RF2: ON)





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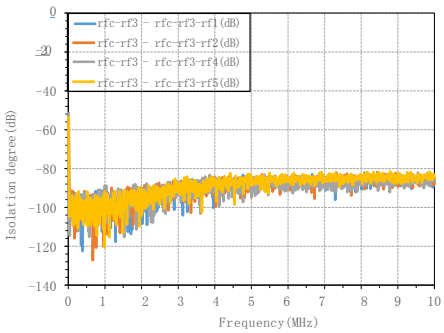
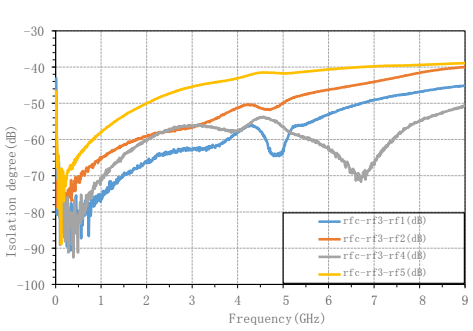
## Test Curve

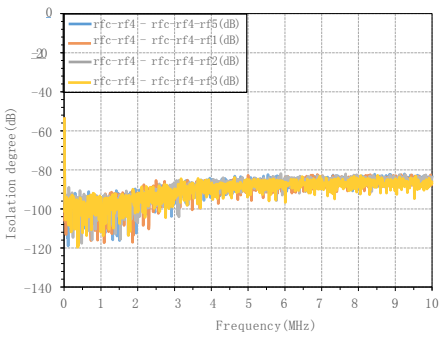
Isolation vs. frequency (10K-10M RF3: ON)



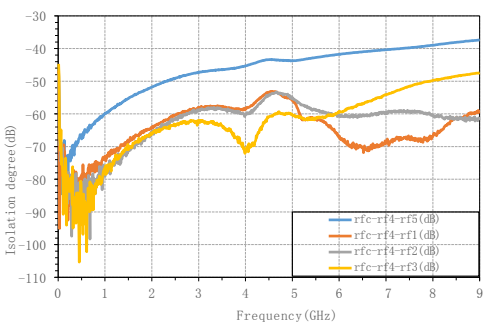

Isolation vs. frequency (10M-9G RF3: ON)



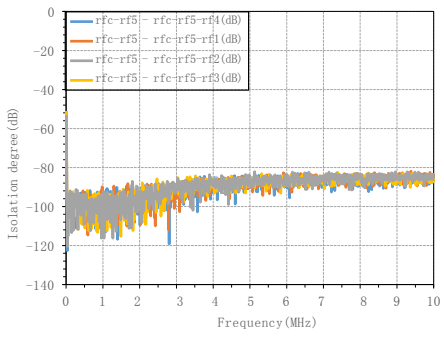

Isolation vs. frequency (10K-10M RF4: ON)



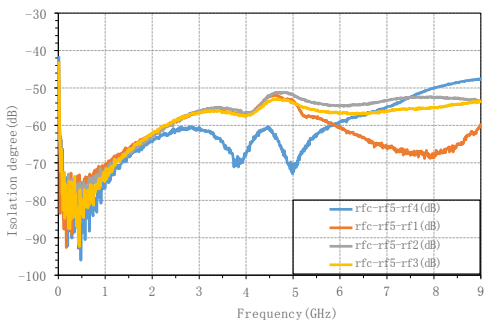

Isolation vs. frequency (10M-9G RF4: ON)




Isolation vs. frequency (10K-10M RF5: ON)

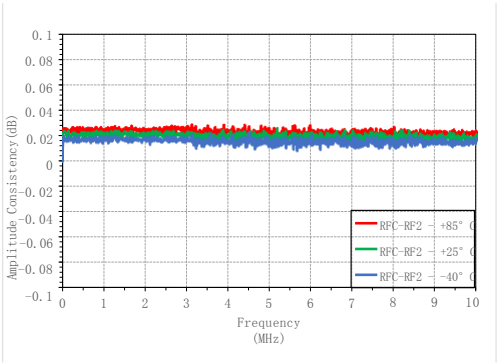



Isolation vs. frequency (10M-9G RF5: ON)

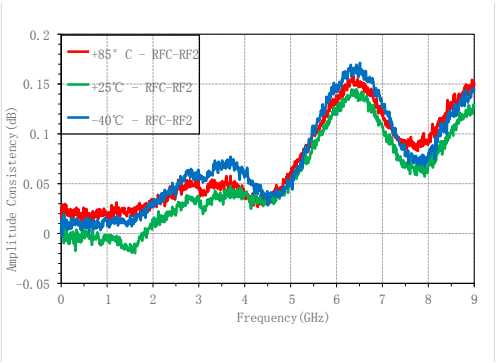


## Test Curve

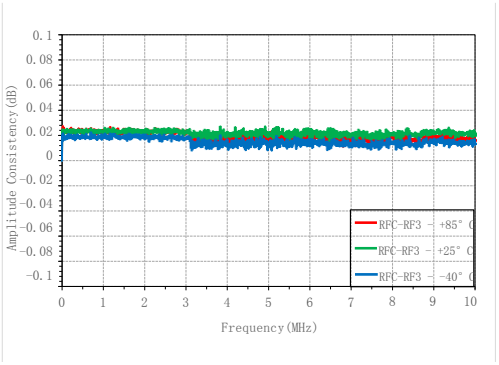
Amplitude Consistency VS Frequency (10K-10M RFC-RF2)



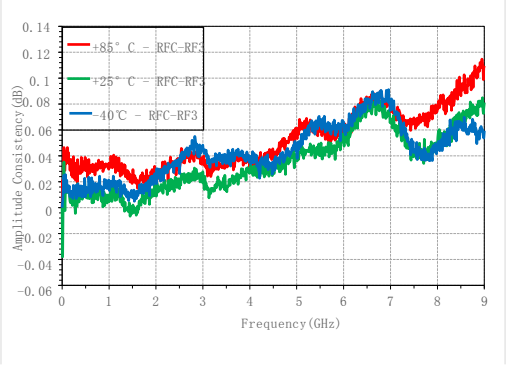

Amplitude Consistency VS Frequency (10M-9G RFC-RF2)



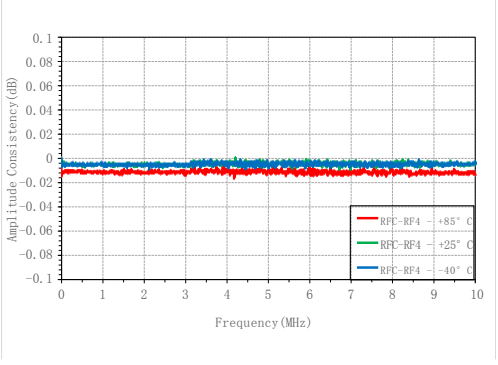

Amplitude Consistency VS Frequency (10K-10M RFC-RF3)



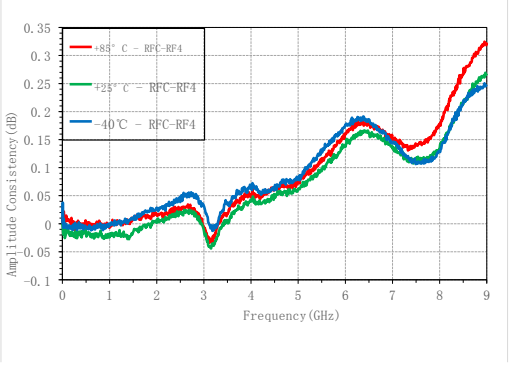

Amplitude Consistency VS Frequency (10M-9G RFC-RF3)




Amplitude Consistency VS Frequency (10K-10M RFC-RF4)




Amplitude Consistency VS Frequency (10M-9G RFC-RF4)





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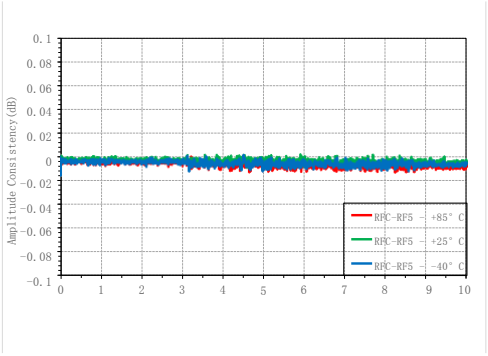
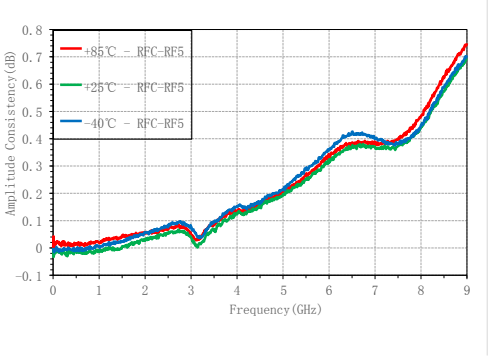
## Test Curve

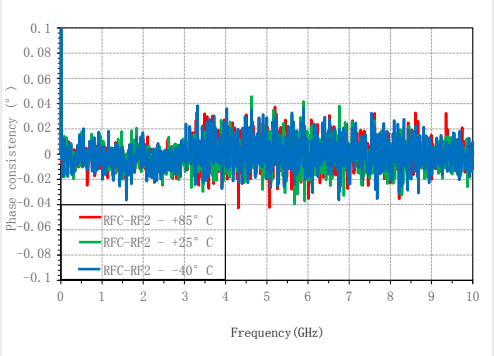
Amplitude Consistency VS Frequency (10K-10M RFC-RF5)



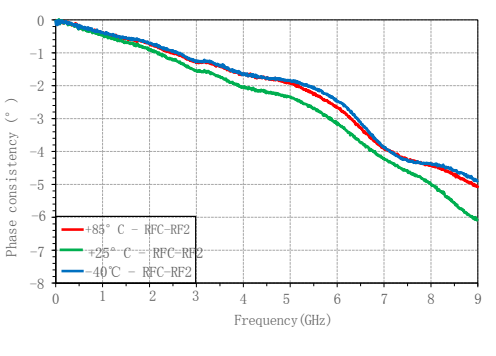

Amplitude Consistency VS Frequency (10M-9G RFC-RF5)



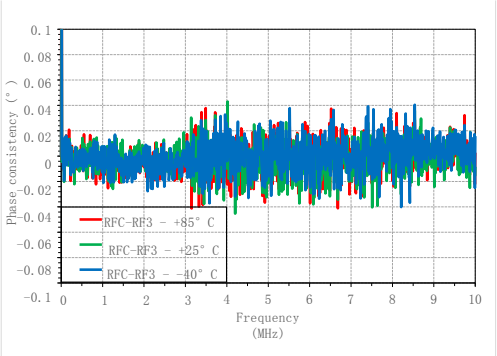

Phase Consistency VS Frequency
(10K-10M RFC-RF2)



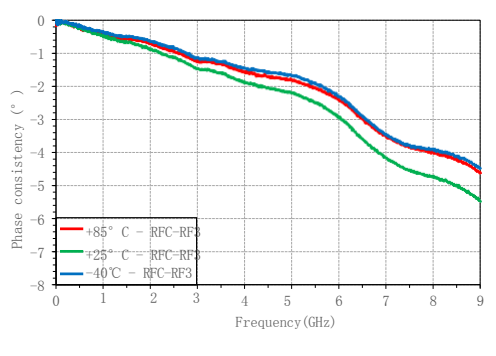

Phase Consistency VS Frequency
(10M-9G RFC-RF2)




Phase Consistency VS Frequency (10K-10M RFC-RF3)

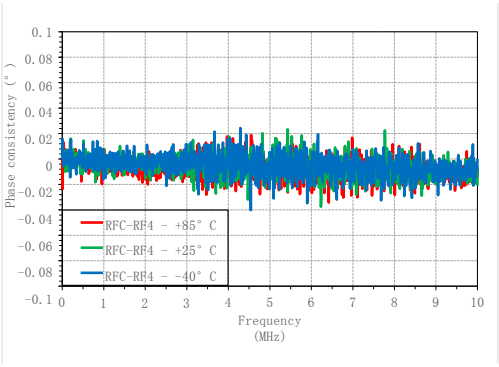



Phase Consistency VS Frequency (10M-9G RFC-RF3)

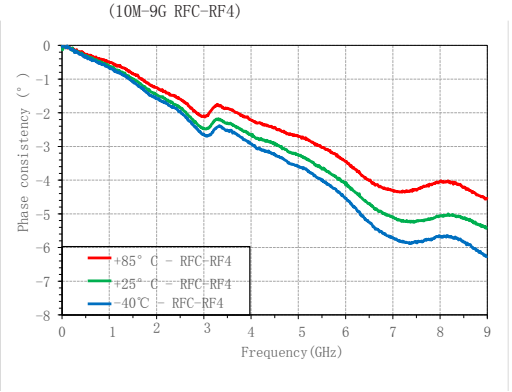


## Test Curve

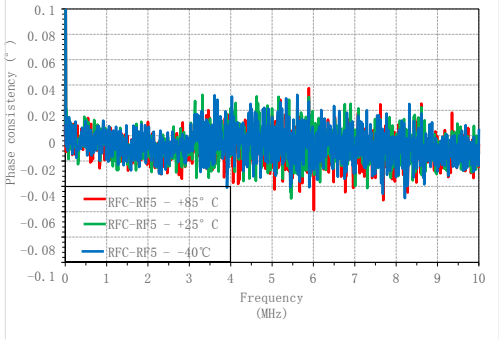
Phase Consistency VS Frequency
(10K-10M RFC-RF4)



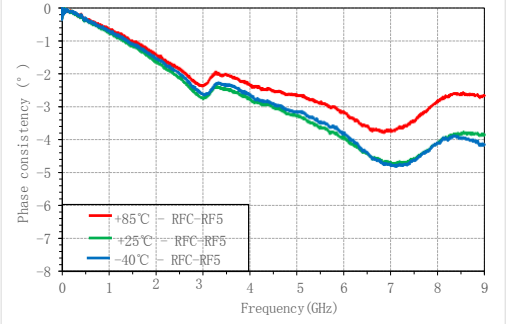

Phase Consistency VS Frequency
(10M-9G RFC-RF4)



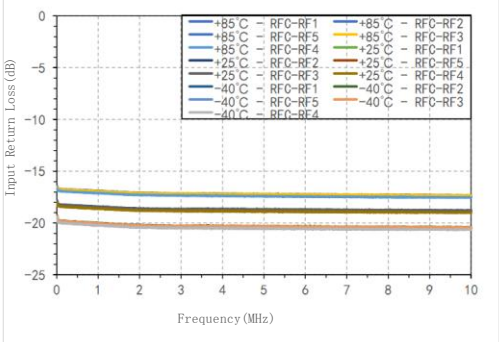

Phase Consistency VS Frequency
(10K-10M RFC-RF5)



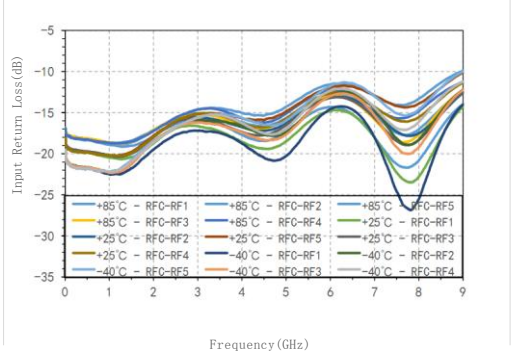

Phase Consistency VS Frequency
(10M-9G RFC-RF5)




Input Return Loss VS
Frequency (10K-10M)




Input Return Loss VS
Frequency (10M-9G)





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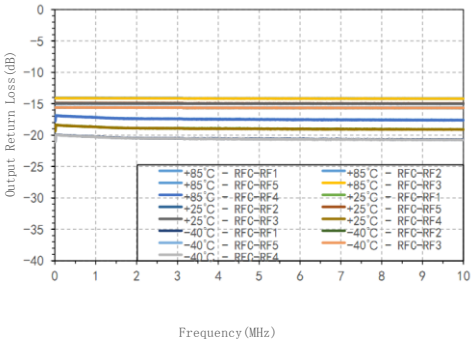
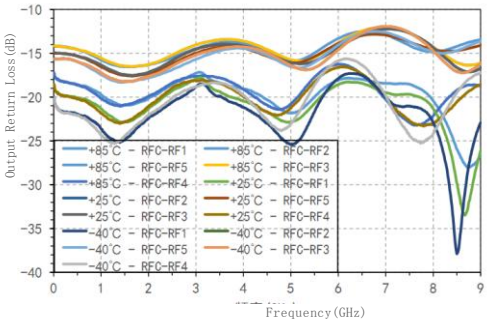
## Test Curve

Output Return Loss VS Frequency (10K-10M)




Output Return Loss VS Frequency (10M-9G)




## Working parameters

| | |
|---|---|
| Bias voltage VDD | 3.0V to 5.0V |
| Control voltage (V1, V2, V3) | 0V～0.3V (Low)<br>VDD-0.3 to VDD (High) |
| Power negative/ground terminal (VSS/GND) | -2.4V to -2V |
| | 0V |
| Operating temperature | -40℃～+85℃ |
| Note: If VSS/GND is connected to -2.4V~-2V, the internal linear voltage regulator is enabled; if it is connected to 0V, the internal voltage generator is enabled. Please select the specific connection method according to the actual situation. | |

## Absolute maximum rating

| | |
|---|---|
| Bias voltage VDD | 6V |
| Control voltage VTRL | VDD+0.3V |
| Input power (insertion loss state) | 32dBm |
| Input power (isolated state) | 32dBm |
| Storage temperature | -65℃～+150℃ |
| Control/Power Port ESD(HBM) | 1000V |
| RF Port ESD(HBM) | 500V |



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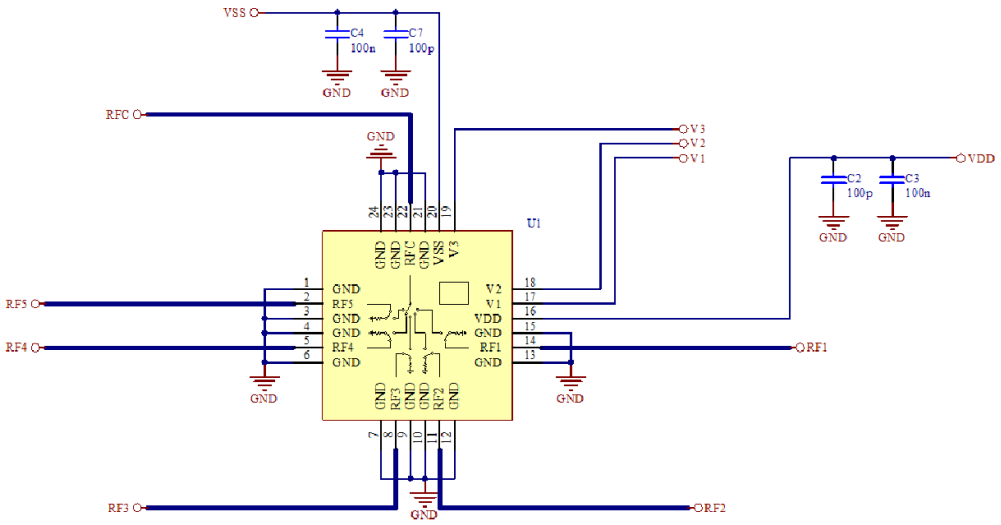
## Package Information

| Model | Packaging Materials | Solder plate plating | MSL level [1] | Package identification [2] | Environmental requirements |
|---|---|---|---|---|---|
| CWS128SP4 | Green resin compounds | NiPdAuAg | MSL 3 | S128<br>XXXXX | RoHS compliant |

[1] Maximum reflow temperature 260° C
[2] XXXXX is the lot number

## Recommended Application Chart





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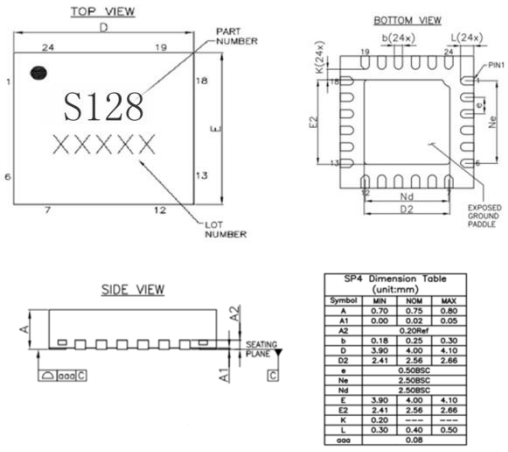
## Dimension




SP4 Dimension Table (unit:mm)

| Symbol | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A2 | | 0.20Ref | |
| b | 0.18 | 0.25 | 0.30 |
| D | 3.90 | 4.00 | 4.10 |
| D2 | 2.41 | 2.56 | 2.66 |
| e | | 0.50BSC | |
| Ne | | 2.50BSC | |
| Nd | | 2.50BSC | |
| E | 3.90 | 4.00 | 4.10 |
| E2 | 2.41 | 2.56 | 2.66 |
| K | 0.20 | ---- | ---- |
| L | 0.30 | 0.40 | 0.50 |
| aaa | | 0.08 | |

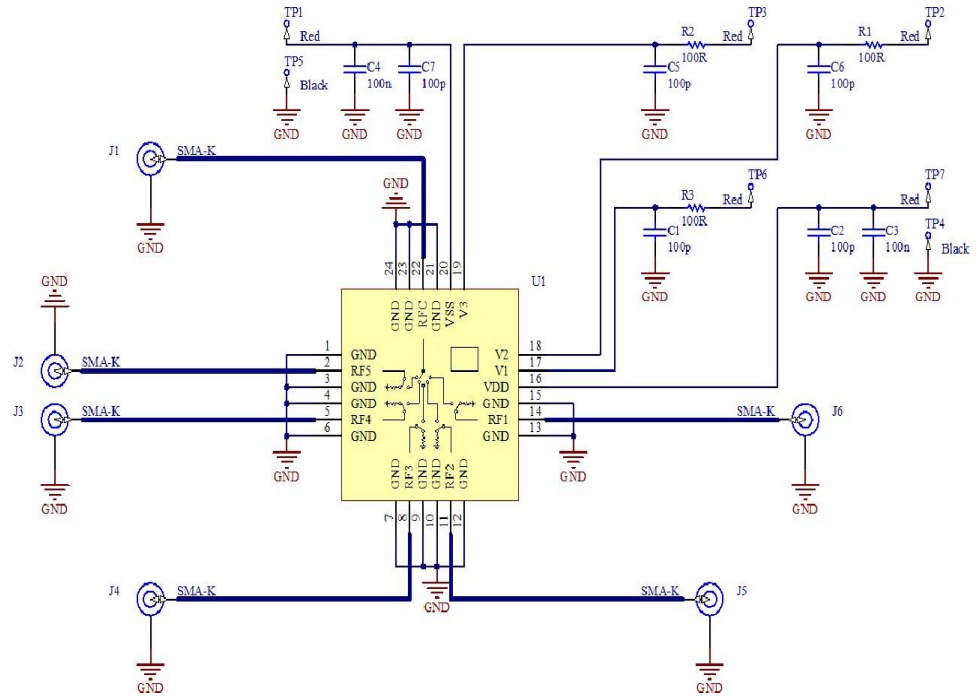
## Pin Definition

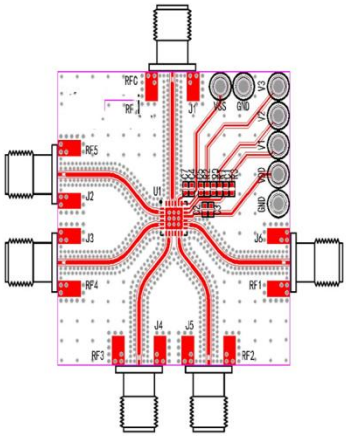
| Pin Number | Function Symbols | Function Description | Schematic diagram |
|---|---|---|---|
| 1; 3-4; 6-7; 9-10; 12-13; 15; 21; 23-24 | GND | RF ground, the bottom of the package exposed paddle is also RF & DC RF ground | GND |
| 2; 5; 8; 11; 14 | rf5; rf4; rf3; rf2; rf1 | RF 5-1 port, DC coupling and matching 50Ω resistor, if the RF side of the potential is not equal to 0V, then you need to isolate the capacitor. | |
| 17 | V1 | Control port 1 | |
| 18 | V2 | Control port 2 | |
| 19 | V3 | Control port 3 | |
| 16; 20 | VDD; VSS | Positive supply voltage port; negative supply voltage port (or ground) | |
| 22 | RFC | RF common port, DC coupling and with 50Ω resistor, if the RF terminal potential is not equal to 0Vdc, then you need to isolate the capacitor. | |

## Truth Table

| Control Input | | | Mode |
|---|---|---|---|
| V1 | V2 | V3 | Of Signal Path |
| 0 | 0 | 0 | ALL OFF; RFC Reflective; RFX Terminated |
| 1 | 0 | 1 | RF1 |
| 0 | 0 | 1 | RF2 |
| 1 | 1 | 0 | RF3 |
| 0 | 1 | 0 | RF4 |
| 1 | 0 | 0 | RF5 |
| 0 | 1 | 1 | ALL OFF; RFC Reflective; RFX Terminated |
| 1 | 1 | 1 | |

## Evaluation Boards



| Designator | Description |
|---|---|
| C3, C4 | Multilayer Ceramic Capacitor 0402 100pF |
| c1, c2, c5, c6, c7 | Multilayer Ceramic Capacitor 0402 100pF |
| R1, R2, R3 | Resistor 0402 100Ω |
| j1, j2, j3, j4, j5, j6 | SMA-K PCB connectors |
| TP1, TP2, TP3, TP4, TP5, TP6, TP7 | DC test terminal |
| U1 | CWS128SP4 |
| J1, J2, J3, J4, J5, J6 recommended to use Nanjing Aowen D550B12E01-032 type SMA-K connector. | |





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