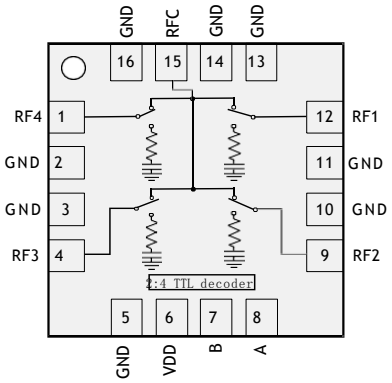
Performance Features

- Operating frequency band: 0.1GHz～6GHz
- Low insertion loss: 0.8dB~1.4dB typical
- High isolation: 65dB@0.1GHz~2GHz
  55dB@2GHz～4GHz
  42dB@4GHz～6GHz
- Package size: 16-pin QFN, 3mmx3mm

Typical Applications

- Base station communication
- Wireless Infrastructure
- Automotive Electronics
- Instrumentation

Functional Block Diagram



Overview

The CWS085SP3 is a highly isolated, low insertion loss, and highly linear single-blade, four-throw switch.

The CWS085SP3 switch is available in a 16-pin 3mmx3mm surface mount leadless plastic package. The pin pad plating is Sn or NiPdAu.

Electrical performance table (TA=+25℃, VDD=3.3V)

Parameter Name	Test conditions	Minimum value	Typical values	Maximum value	Unit
RF Frequency Range		0.1 to 6			GHz
insert loss	0.1GHz～2GHz		0.8	1.2	dB
	2GHz～4GHz		1.1	1.4	dB
	4GHz～6GHz		1.4	1.9	dB
Isolation	0.1GHz～2GHz		50		dB
	2GHz～4GHz		40		dB
	4GHz～6GHz	28	33		dB
Return loss	open state		20		dB
	Off-state		20		dB
Bias Voltage (VDD)		3	3.15	3.3	V
Bias Current (IDD)				1	mA
Input 0.1dB compression point power (P0.1dB)	open state		26		dBm
Input 1dB compression point power (P1dB)	open state		27.5		dBm
Input third-order intercept point of intersection (IP3)			TBD		dBm
Rise and fall time	10% to 90% RF output		140		ns
Switching time	50% Vctl to 10%/90% RF output		200		ns
Recommended input power	Passage diameter			26	dBm
	final path			26	dBm

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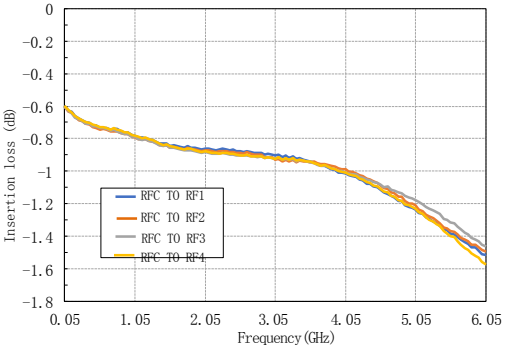
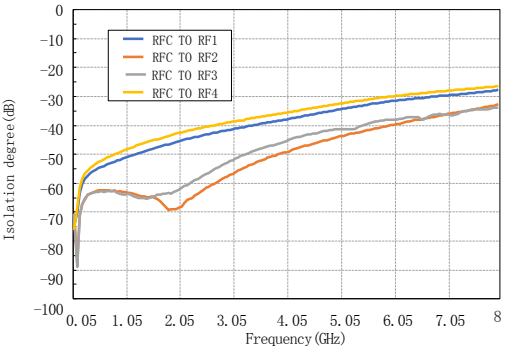
Test Curve

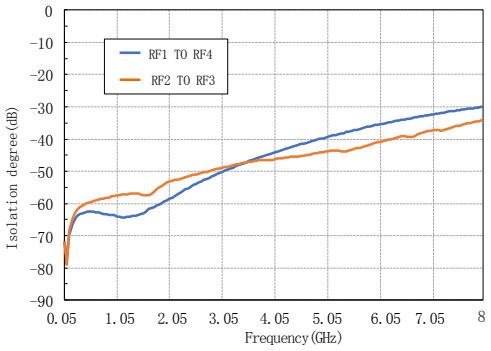
Insertion loss vs. frequency



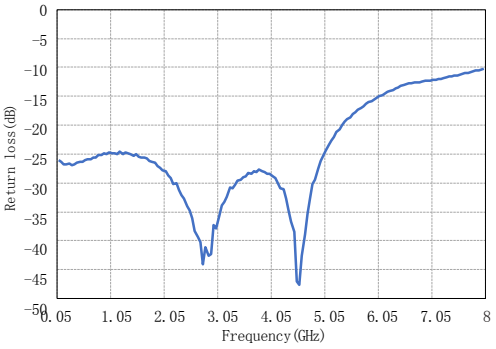
Isolation vs. frequency



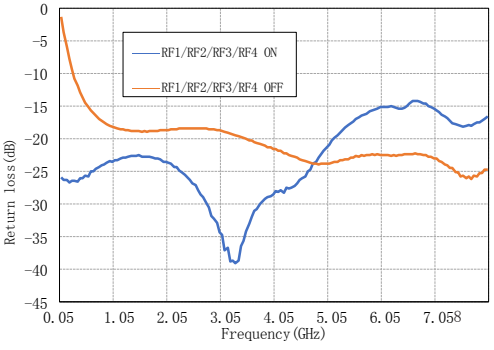
Isolation vs. frequency



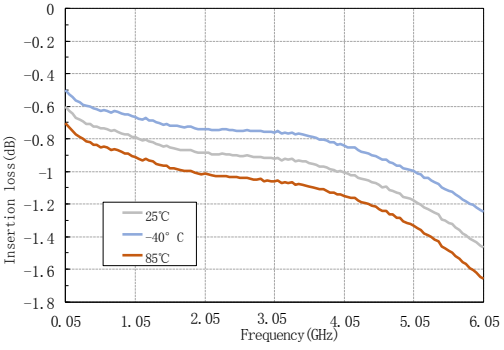
RFC return loss vs. frequency



RFN return loss vs. frequency



Insertion loss vs. frequency



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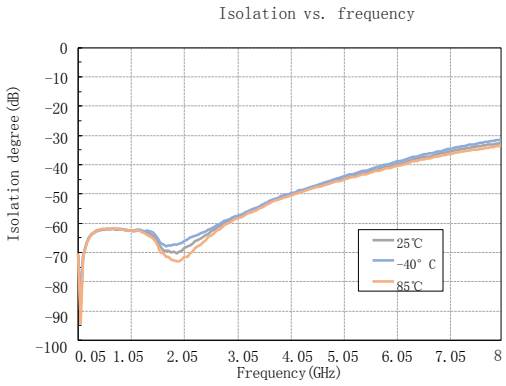
Test Curve



Working parameters

Bias voltage VDD	3V to 3.3V
Control voltage A, B	0V～0.3V (Low) 3V to 3.3V (High)
Operating temperature	-40℃～+85℃

Absolute maximum rating

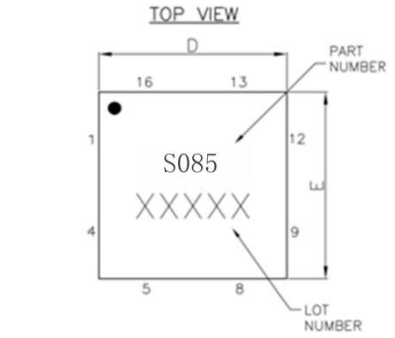
Bias voltage VDD	-0.3V~3.6V
Control voltage EN, VCTL	-0.5 V~VDD+0.3V
Input power (through-hole)	33dBm
Input power (final diameter)	33dBm
Storage temperature	-65℃～+150℃

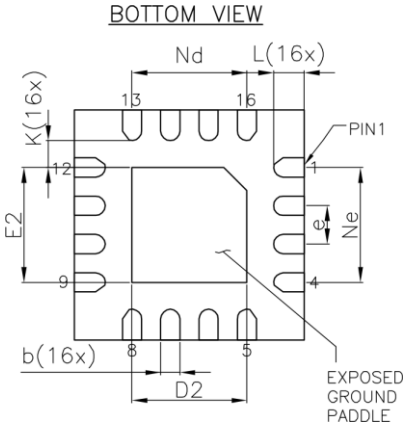
Package Information

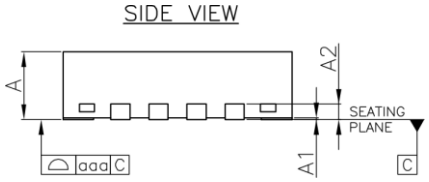
Model	Packaging Materials	Solder plate plating	MSL level [1]	Package identification [2]	Environmental requirements
CWS085SP3	Green resin compounds	Sn or NiPdAu	MSL 3	S085 XXXXX	RoHS compliant

[1] Maximum reflow temperature 260° C
[2] XXXXX is the lot number

Dimension







Description:

1. Unit: mm
2. Lead frame material: copper alloy
3. Package surface warpage: not more than 0.05mm
4. All ground pins please connect PCB RF ground

Dimension Table (unit:mm)			
Symbol	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	---	0.05
A2		0.20Ref	
b	0.20	0.25	0.30
D	2.90	3.00	3.10
D2	1.40	1.50	1.60
e		0.50BSC	
Ne		1.50BSC	
Nd		1.50BSC	
E	2.90	3.00	3.10
E2	1.40	1.50	1.60
K	0.20	---	---
L	0.30	0.40	0.50
aaa		0.08	

Pin Definition

Pin Number	Function Symbols	Function Description	Pin Number	Function Symbols	Function Description
1	RF4	RF 4-Port	9	RF2	RF 2 ports
2	GND	RF Ground	10	GND	RF Ground
3	GND	RF Ground	11	GND	RF Ground
4	RF3	RF 3-Port	12	RF1	RF 1 port
5	GND	RF Ground	13	GND	RF Ground
6	VDD	Bias voltage	14	GND	RF Ground
7	B	Control B port	15	RFC	RF Common Side
8	A	Control A port	16	GND	RF Ground

All NC pins are recommended to be connected to RF ground when in use

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Truth Table

Control and bias inputs			Signaling pathway status
Bias Voltage (VDD)	Control A port	Control B port	
3.3V	Low	Low	RFC to RF1
3.3V	High	Low	RFC to RF2
3.3V	Low	High	RFC to RF3
3.3V	High	High	RFC to RF4

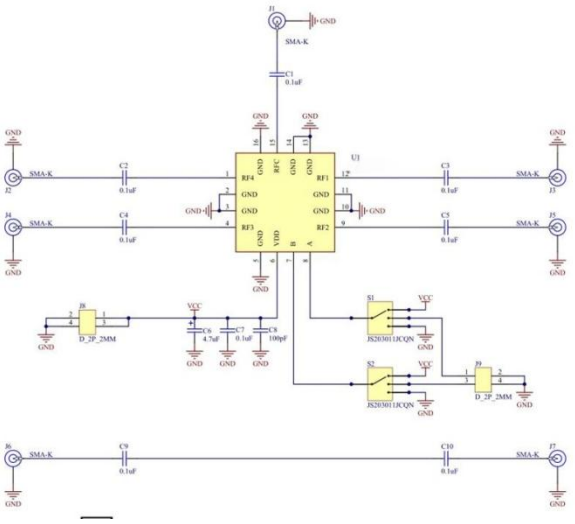
Working Principle

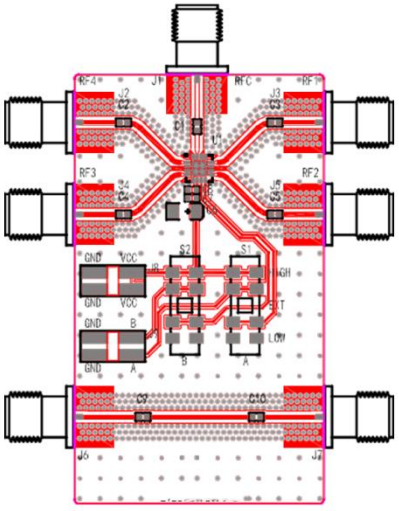
1. This switch requires a supply voltage to be applied to the VDD pin. It is recommended to bypass the capacitor on the power line to minimize RF coupling.
2. A 2:4 compiler is integrated inside this switch and the four RF paths are selected by two digital control voltages applied to the A and B control inputs. It is recommended to install a small bypass capacitor on these digital signal lines to improve the isolation of the RF signals.
3. The RF common port (RFC) and the RF output ports (RF1, RF2, RF3, RF4) are internally matched with 50Ω, so no external matching is required. The RF pins are direct-coupled, and the RF terminals need to be peripherally equipped with isolation capacitors. The design is bi-directional and the RF input signal can be applied to either the RFC port or the RF1 to RF4 port. The inputs and outputs are interchangeable.
4. Depending on the logic levels applied to the control input pins A and B, one RF output port (e.g., RF1) is set to open mode, which provides an insertion loss path from the input to the output. The other RF output ports (e.g., RF2, RF3, and RF4) are then set to the off mode, through which the output is isolated from the input. When the RF output ports (RF1, RF2, RF3, and RF4) are in isolated mode, they are internally terminated to 50 Ω so that they can absorb the applied RF signal.

Recommended power supply sequence

1. GND is energized.
2. VDD is energized.
3. Turn on the digital control inputs. The relative order of the digital control inputs is not important. Turning on the digital control inputs before the VDD power supply may inadvertently cause bias and damage the ESD protection structure.
4. Turn on the RF input.

Evaluation Boards





Designator	Description
c1, c2, c3, c4, c5, c9, c10	0.1uF Ceramic Capacitor 0402
C6	4.7uF Tantalum Capacitor 3216
C7	0.1uF Ceramic Capacitor 0402
C8	100pF Ceramic Capacitor 0402
j1, j2, j3, j4, j5, j6, j7	SMA PCB connector
J8, J9	4Pin DC pins
S1, S2	Toggle Switch
U1	CWS085SP3
J1, J2, J3, J4, J5 recommended to use Nanjing Aowen D550B12E01-048 type SMA Connectors	

Circuit board material: Rogers 4350B

The circuit board of the device application should be designed in accordance with the RF circuit design method, the signal line is designed according to 50Ω impedance, while the grounding pin of the package shell is grounded nearby (similar to the figure), connecting the top and bottom ground should have enough grounding holes.

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