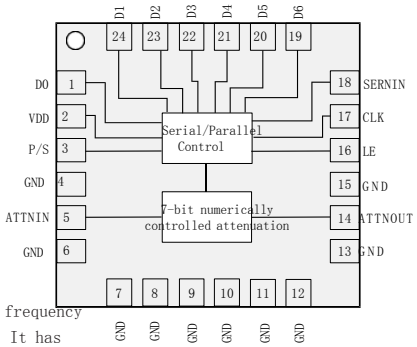
Performance Characteristics

- Operating frequency band: 0.1GHz～8GHz
- Low insertion loss: 0.5dB @0.1GHz to 2GHz (typ)
  0.9dB @2GHz to 4GHz(typ) 1.4dB @4GHz to 6GHz(typ) 1.7dB @6GHz to 8GHz(typ)
- Attenuation range: 0.25dB ~ 31.75dB
- Package Size: 24-pin QFN, 4mmx4mm

typical application

- Mobile infrastructure
- satellite communications
- microwave
- Instrumentation

functional block diagram



summarize

The CWAT4002SP4 is a seven-bit numerically controlled attenuator with a frequency range of 0.1 GHz to 8 GHz and an insertion loss of less than 1.7 dB typical. It has high attenuation accuracy, 0.25 dB attenuation step, and 3.3V bias voltage.

The CWAT4002SP4 attenuator is available in a 24-pin, 4mmx4mm surface mount, leadless plastic package. The pin pads are coated with Sn or NiPdAu.

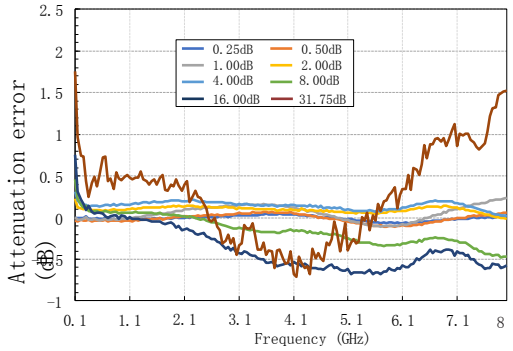
Electrical performance table (TA=+25°C, VDD=3.3V)

Parameter name	working conditions	minimum value	typical value	maximum values	unit (of measure)
frequency range		0.1		8	GHz
insertion loss	0.1GHz~2GHz		0.5	0.8	dB
	2GHz~4GHz		0.9	1.4	dB
	4GHz~6GHz		1.4	1.9	dB
	6GHz~8GHz		1.7	2.1	dB
Attenuation range	0.1GHz~8GHz		31.75		dB
Attenuation accuracy	0.1GHz~6GHz	-0.5		0.8	dB
	6GHz~8GHz	-0.6		1.6	dB
Input and output return loss			18		dB
Bias Voltage (VDD)		3	3.15	3.3	V
Bias Current (IDD)				1	mA
0.1dB compression point input power (P0.1dB)			24		dBm
1dB Compression Point Input Power (P1dB)			31		dBm
Input third-order intercept point (interpolated/attenuated state)	Pin=10dBm@1MHz		55/45		dBm
Switching time (insertion loss state to maximum attenuation state)	10% to 90% RF output		240		ns
Switching time (maximum attenuation state to insertion loss state)	10% to 90% RF output		100		ns
switching time	50% Vctl to 10%/90% RF output		220		ns
Recommended Input Power				30	dBm

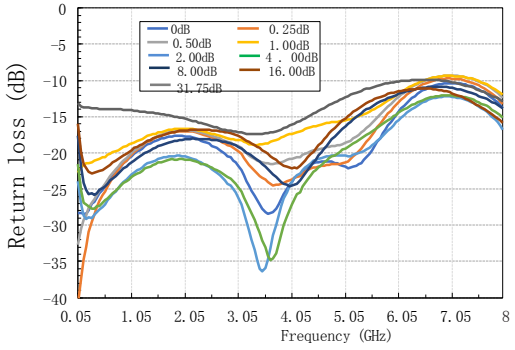
Note: There is no isolation capacitor on the RF port of this chip, the RF port of the chip has voltage, and isolation capacitor must be added when the chip is cascaded with other devices.

test curve

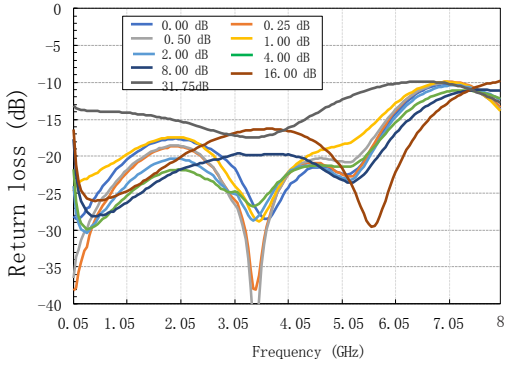
Attenuation error vs. frequency



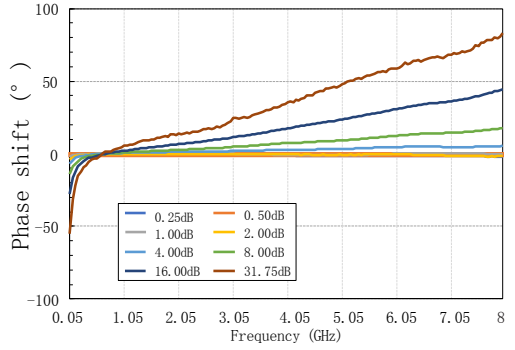
Input return loss vs. frequency



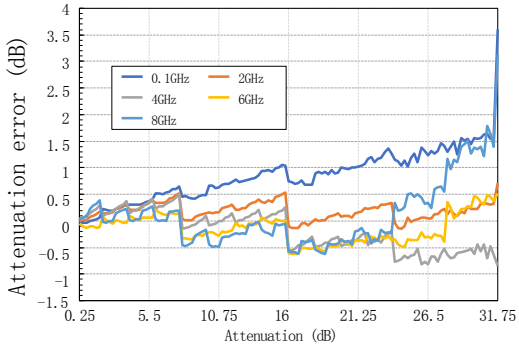
Output return loss vs. frequency



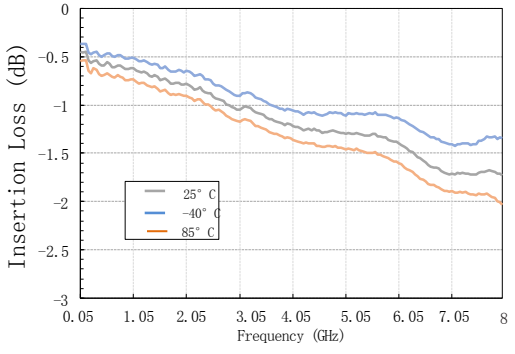
Phase Shift VS Frequency



Attenuation Error vs.

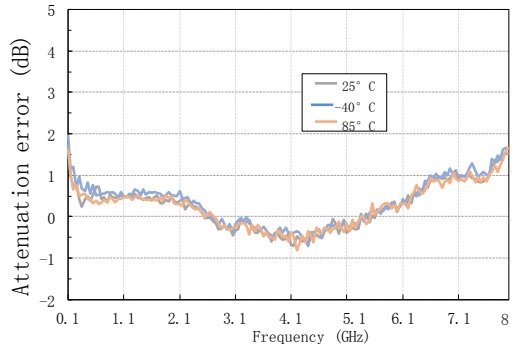


Insertion Loss vs. Frequency

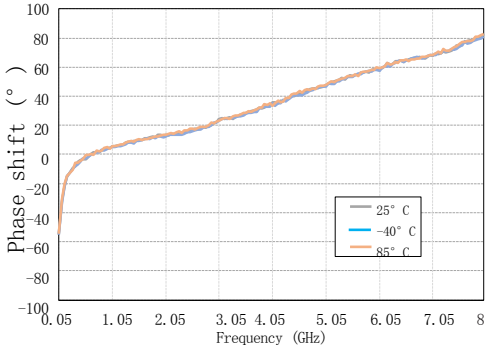


test curve

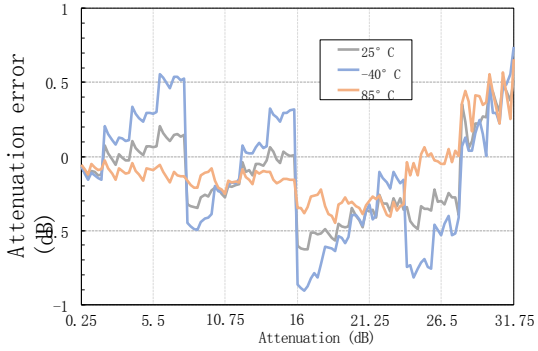
Attenuation error VS frequency @ 31.75dB



Phase shift VS frequency @ 31.75dB



Attenuation Error vs Attenuation @ 6GHz



Operating parameters

Bias voltage VDD	3V to 3.3V
Control voltage VCTL	0V to 0.3V (Low) 3V to 3.3V (High)
operating temperature	-40℃～+85℃
ESD (HBM)	Class 1C

Control Port: D0~D6, P/S, LE, CLK, SERNIN

Absolute maximum rating

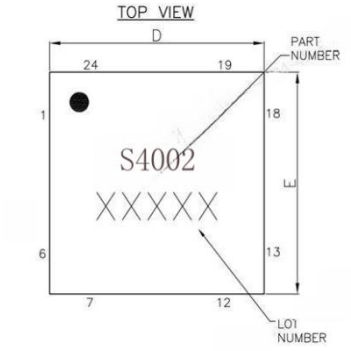
RF Input Power	+32dBm
Bias Voltage VDD	-0.3V~3.6V
Control Voltage VCTL	-0.5 V~VDD+0.3V
Storage temperature	-65℃～+150℃

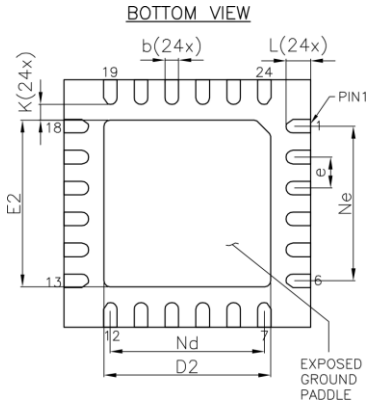
Package Information

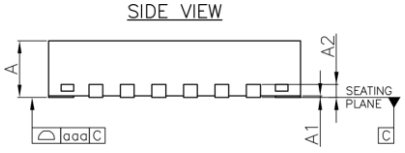
model number	package material	Pad plating	MSL rating [1]	Package identification [2]	environmental requirement
CWAT4002SP4	Green resin compounds	Sn or NiPdAuAg	MSL 3	S4002 XXXXX	RoHS compliant

[1] Maximum reflow temperature 260° C
[2] XXXXX is the lot number

Overall dimensions







Description:

1. Unit: mm
2. Lead frame material: copper alloy
3. Package surface warpage: not more than 0.05mm
4. All ground pins should be connected to PCB RF ground.

Dimension Table (unit:mm)

Symbol	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	---	0.05
A2		0.20Ref	
b	0.20	0.25	0.30
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
e		0.50BSC	
Ne		2.50BSC	
Nd		2.50BSC	
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
K	0.20	---	---
L	0.30	0.40	0.50
aaa		0.08	

Pin Definitions

Pin Number	functional symbol	Functional Description	Pin Number	functional symbol	Functional Description
1	D0	Console 0 port	13	GND	radio-frequency zone
2	VDD	DC Bias	14	ATTNOUT	RF output
3	P/S	serial-to-parallel selector terminal	15	GND	radio-frequency zone
4	GND	radio-frequency zone	16	LE	enabling terminal
5	ATTNIN	RF input	17	CLK	clock side
6	GND	radio-frequency zone	18	SERNIN	Serial Data Input
7	GND	radio-frequency zone	19	D6	Console 6 ports
8	GND	radio-frequency zone	20	D5	Console 5 ports
9	GND	radio-frequency zone	21	D4	Console 4 ports
10	GND	radio-frequency zone	22	D3	Console 3 ports
11	GND	radio-frequency zone	23	D2	Console 2 ports
12	GND	radio-frequency zone	24	D1	Console 1 port

truth table

Control Port Status							Attenuation status (dB)
D6	D5	D4	D3	D2	D1	D0	
Low	Low	Low	Low	Low	Low	Low	zero state (math.)
Low	Low	Low	Low	Low	Low	High	0.25
Low	Low	Low	Low	Low	High	Low	0.5
Low	Low	Low	Low	High	Low	Low	1.0
Low	Low	Low	High	Low	Low	Low	2.0
Low	Low	High	Low	Low	Low	Low	4.0
Low	High	Low	Low	Low	Low	Low	8.0
High	Low	Low	Low	Low	Low	Low	16.0
High	High	High	High	High	High	High	31.75

Any combination of the above states will provide attenuation approximately equal to the sum of the selected bits

Control mode selection

P/S status	control mode
Low	side by side (of two processes, developments, thoughts etc)
High	confuse two lines

The P/S pin must remain in a valid logic state (High or Low) and must not be left floating

Serial control output

The serial control interface is active when the P/S pin is set high.

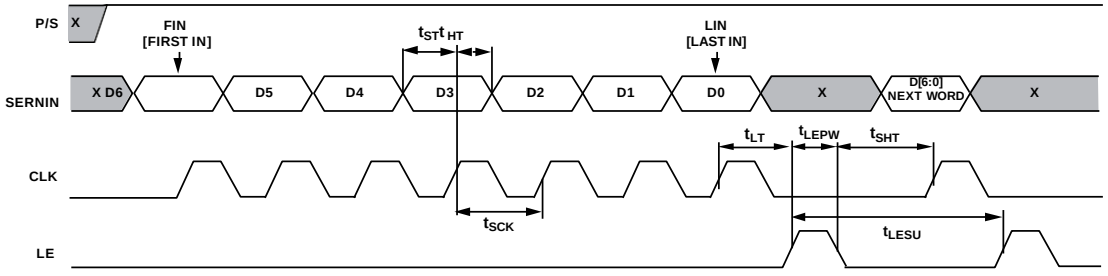
In serial mode, seven bits of serial data are first clocked to the highest bit when the CLK edge rises to the shift register, and then LE must be switched high to latch the new attenuation state. LE must be set low to write a set of seven bits to the shift register, as CLK is masked to prevent the attenuation value from changing while LE remains high.

During serial mode operation, the serial control inputs (LE, CLK, SERNIN) and parallel control inputs (D0 through D6) must be maintained at valid logic levels (High or Low) at all times and must not be left floating. If the device driving these input lines experiences high impedance during sleep, it is recommended that the parallel control inputs be connected to ground and that pull-down resistors be used on all serial control input lines. (See Serial Control Timing Diagram)

RF Input and Output

The attenuator is bi-directional; the ATTNIN and ATTNOUT pins are interchangeable as RF input and output ports. The attenuator is internally matched to 50Ω on the input and output; therefore, no external matching is required. The RF pins are DC coupled; therefore, DC blocking capacitors are required on the RF lines.

Control mode selection



Serial Control Timing Diagram

Parallel control output

The parallel control port has seven digital control inputs (D6 through D0) for setting the attenuation value; D6 is the highest valid bit for selecting 16 dB attenuation, and D0 is the lowest valid bit for selecting 0.25 dB attenuation.

During parallel mode operation, the serial control inputs (LE, CLK, SERNIN) and parallel control inputs (D0 through D6) must always be maintained at a valid logic level (High or Low) and must not be left floating. If the devices driving these input lines have high impedance during sleep, it is recommended that the serial control inputs be connected to ground and that pull-down resistors be used on all parallel control input lines.

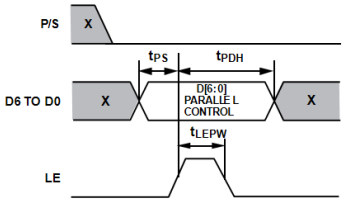
Parallel mode is enabled by setting P/S low. There are two modes of parallel operation: direct parallel mode and latching parallel mode.

direct parallelism

For direct parallel mode, LE must be held high. The attenuation state is changed directly using the control voltage inputs (D0 through D6). This mode is ideal for manually controlling the attenuator and using hardware, switches or jumpers.

Latch Parallel Mode

When changing the control voltage inputs (D0 through D6) to set the attenuation state, the LE port must be held low. To set the desired state, LE must be switched to High to transmit the 7-bit data to the attenuator array's bypass switch, and then switched to Low to latch the changes into the device. (See Latch Parallel Mode Timing Diagram)



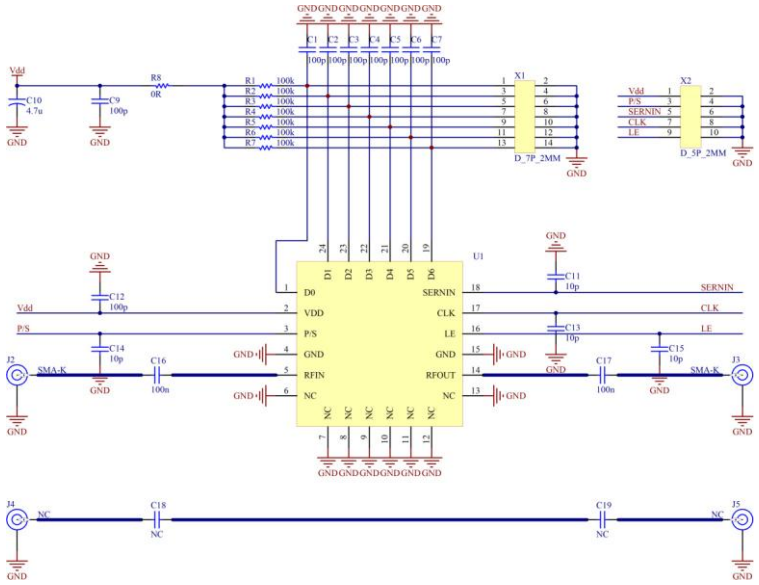
Latch Parallel Mode Timing Diagram

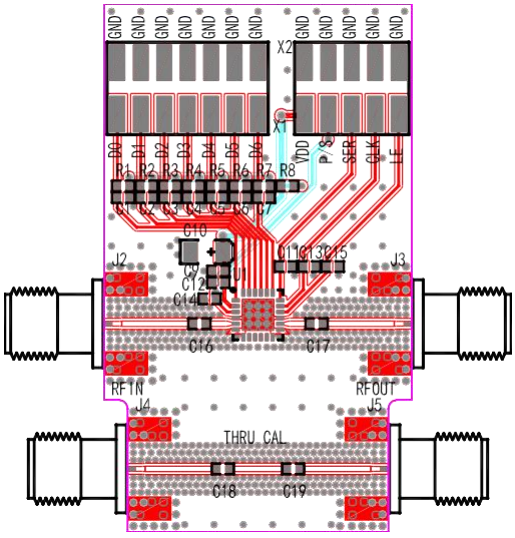
Power-up sequence and status

1. GND is energized.
2. VDD energized.
3. Turn on the digital control inputs (the relative order of the digital control inputs is not important).
4. Turn on the RF input.
5. For latched parallel mode, the LE must be switched. the relative order of the digital inputs does not matter as long as the inputs are energized after ground and VDD.

When energized, the logical state of the unit is maximum attenuation when LE is set to low. The attenuator locks at the desired energized state after approximately 200ms of energization.

evaluation board





DeCWgnator	Description
c1, c2, c3, c4, c5. C6, C7, C9, C12	Multilayer Ceramic Capacitors 0402 100pF
C16, C17	Multilayer Ceramic Capacitors 0402 100nF
C10	Tantalum Capacitor 3216 4.7uF
C11, C13, C14, C15	Multilayer Ceramic Capacitors 0402 10pF
r1, r2, r3, r4, r5. R6, R7	Resistance 0402 100kΩ
R8	Resistor 0402 0Ω
J2, J3	SMA-K PCB Connectors
X1, X2	2.0mm DC Pin
U1	CWAT4002SP4
J2, J3 Recommended to use Nanjing Aowen D550B12E01-023 SMA-K with connectors	
NC indicates an unused port or the device is not soldered. The NC port of the chip can be externally connected to GND.	