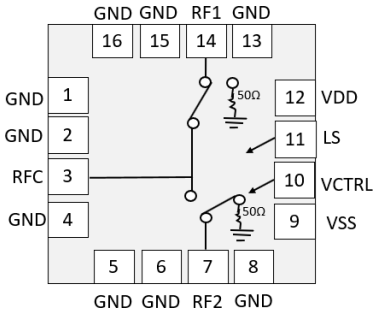
Performance Characteristics

- Operating frequency band: DC ~ 13GHz
- Low insertion loss: 0.8dB typical @ 10K to 6GHz
- High isolation: 50dB@10K~6GHz
  38dB@6GHz~8GHz
  30dB@8GHz~13GHz
- Package Size: 16-pin QFN, 3mmx3mm

typical application

- base station communication
- wireless infrastructure
- automotive electronics
- Instrumentation

functional block diagram



summarize

The CWS110ASP3 is a high isolation, low insertion loss, high linearity single-pole, double-throw switch.
The CWS110ASP3 switches are available in a 16-pin, 3mmx3mm surface mount, leadless plastic package. The pin pads are coated with Sn or NiPdAu.

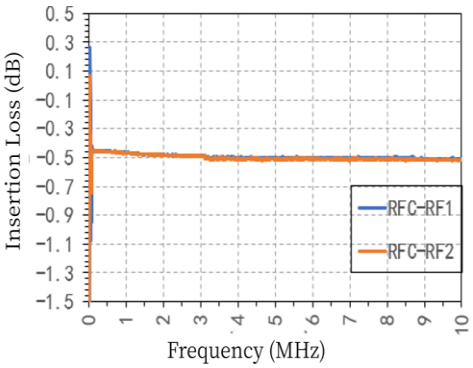
电性能表 (TA=+25℃, V_{CTRL}=0/3.3V, VSS=-2.4V, VDD=LS=3.3V)

Parameter name	test condition	minimum value	typical value	maximum values	unit (of measure)
RF Frequency Range			DC ~ 13		GHz
insertion loss	10K to 6GHz		0.8		dB
	6GHz to 8GHz		1.2		dB
	8GHz to 13GHz		1.8		dB
incommunicado	10K to 6GHz		50		dB
	6GHz to 8GHz		38		dB
	8GHz to 13GHz		30		dB
return loss	open state (math.)		-15		dB
	camouflage		-10		dB
phase coherence			0	1.5	
Amplitude consistency			0	0.1	dB
Bias Voltage (VDD)		3		5.3	V
Bias Current (IDD)				1	mA
Rise and fall time	10% to 90% RF output		30		ns
switching time	50% VCTRL to 10%/90% RF output		120		ns
Recommended Input Power	plug-in mode (math.)			31	dBm
	segregated state (physics)			26	dBm

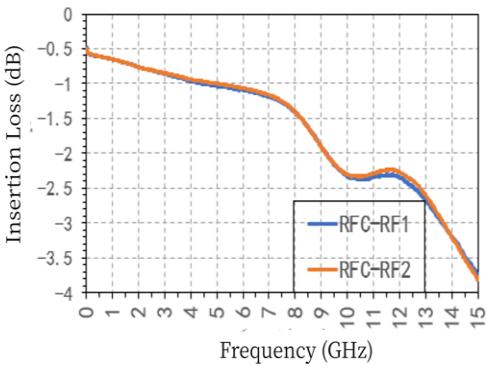
Note: 1. The lowest frequency of the test instrument to 10K, so only display 10K above the test data
2. The chip does not have an integrated DC/DC converter module, so the chip positive/negative power (VDD/VSS) must be added to the VSS range of -2.0 ~ -2.4 (V)

test curve

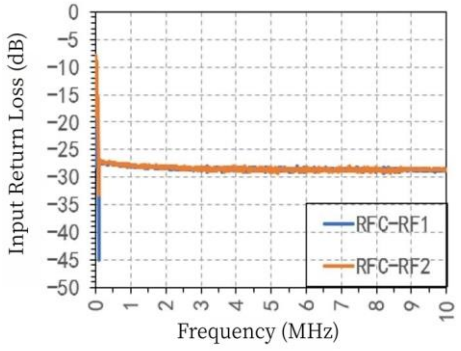
Insertion Loss vs. Frequency (@10K-10MHz)



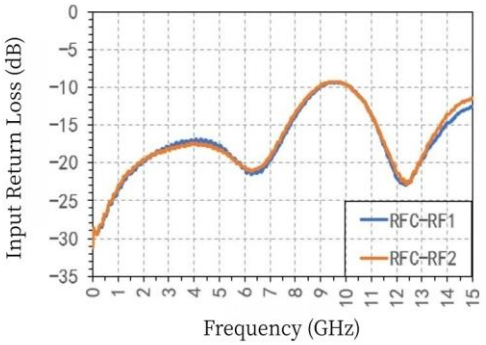
Insertion loss vs. frequency (@10M-15GHz)



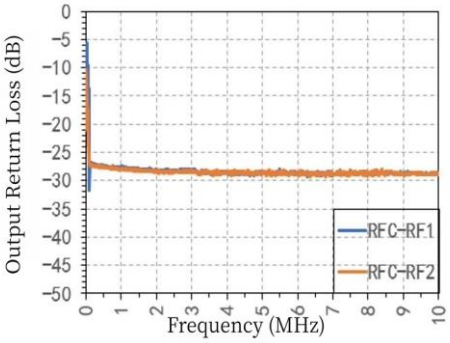
Input Return Loss VS Frequency (@10K-10MHz)



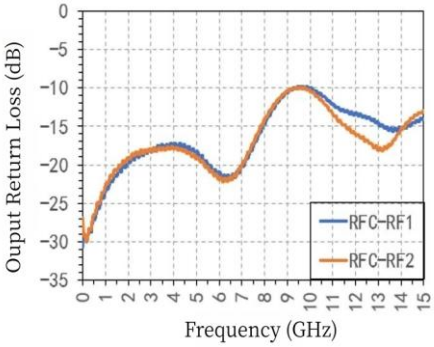
Input return loss vs. frequency (@10M-15GHz)



Output return loss vs. frequency (@10K-10MHz)



Output return loss vs. frequency (@10M-15GHz)



CWS

Switch Regulator Series

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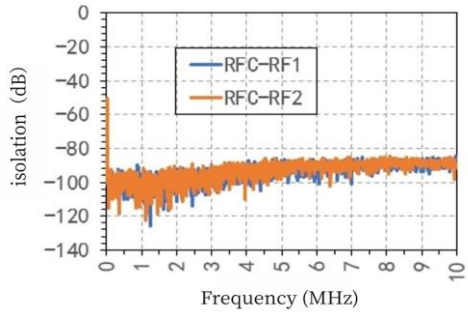
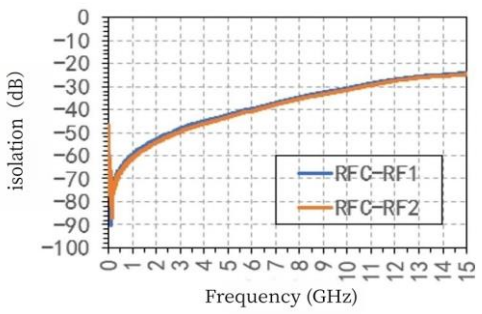
test curve

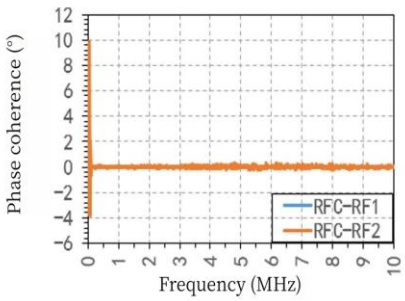
Isolation vs. Frequency (@10K-10MHz)



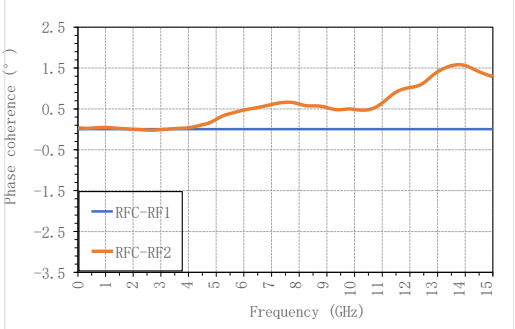
Isolation vs. Frequency (@10M-15GHz)



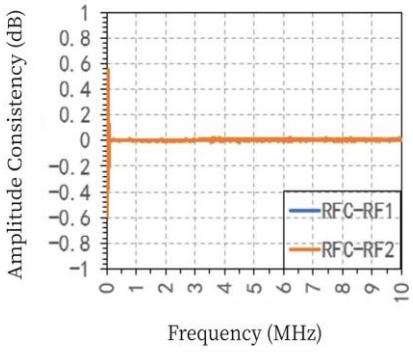
Phase coherence vs. frequency (@10K-10MHz)



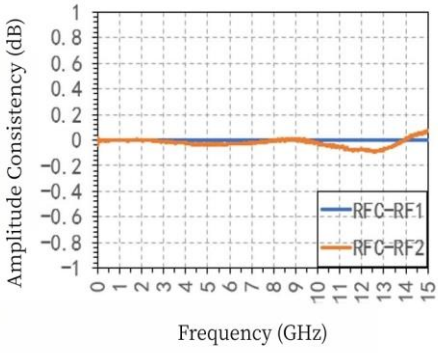
Phase coherence vs. frequency (@10M-15GHz)



Amplitude consistency vs. frequency (@10K-10MHz)



Amplitude consistency vs. frequency (@10M-15GHz)



Operating parameters

Negative power supply VSS	-2V to 2.4V
Bias voltage VDD	3V to 5.3V
Control voltage LS, VCTRL	0V to 0.3V (Low) 3V to 5.0V (High)
operating temperature	-45℃～+85℃

Absolute maximum rating

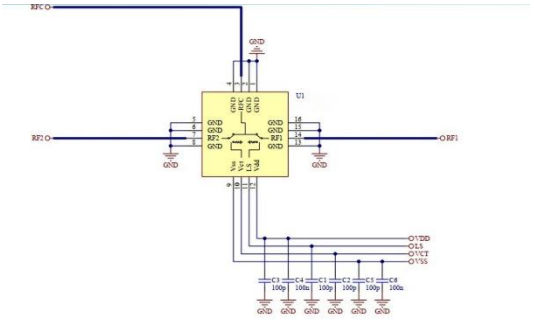
Bias Voltage VDD	-0.3V/5.6V
Control Voltage LS, VCTRL	-0.5 V/VDD+0.3V
Input power (insertion loss state)	33dBm
Input power (isolated state)	31dBm
Storage temperature	-65℃～+150℃

Package Information

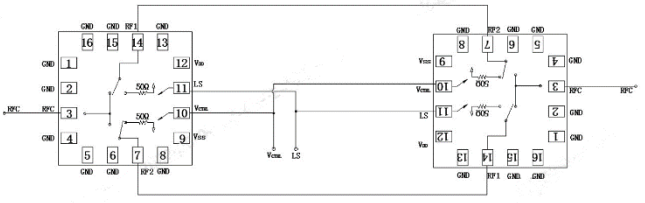
model number	package material	Pad plating	MSL rating [1]	Package identification [2]	environmental requirement
CWS110ASP3	Green resin compounds	Sn or NiPdAu	MSL 3	S110A XXXXX	RoHS compliant

[1] Maximum reflow temperature 260° C
[2] XXXXX is the lot number

Typical Application Circuit Diagram



mirroring application



CWS110ASP3

Control Input		Signal Path State	
LS	VCTRL	RFC to RF1	RFC to RF2
High	Low	Off	On
High	High	On	Off
Low	Low	On	Off
Low	High	Off	On

CWS110SP3

Control Input		Signal Path State	
LS	VCTRL	RFC to RF1	RFC to RF2
High	Low	On	Off
High	High	Off	On
Low	Low	Off	On
Low	High	On	Off

Since the switches CWS110ASP3 and CWS110SP3 switcheshave opposite logic controls, for applications where a pair of switches is required (e.g., applications such as switched filter banks), the control wires can be directly connected for ease of use.

Chengdu Cuiwei Electronic Co.,LTD
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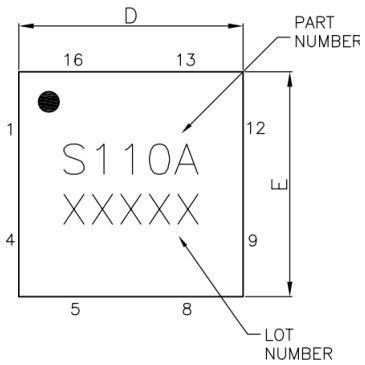
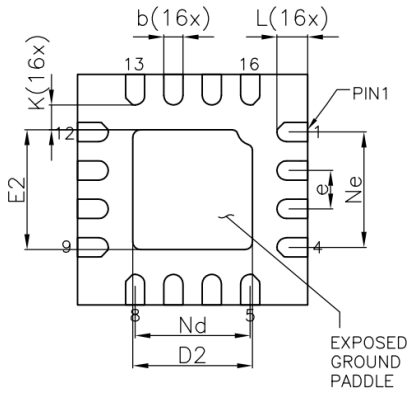
Website: www.cdcwtec.com

Overall dimensions

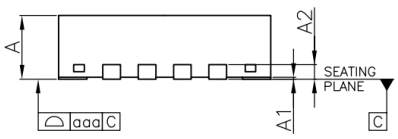
TOP VIEW



BOTTOM VIEW



SIDE VIEW



Description:
1. Unit: mm
2. Lead frame material: copper alloy
3. Package surface warpage: ≤ 0.05mm
4. All ground pins should be connected to PCB RF ground.

SP3 Dimension Table (unit:mm)

Symbol	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.20Ref	
b	0.18	0.25	0.30
D	2.90	3.00	3.10
D2	1.41	1.56	1.70
e		0.50BSC	
Ne		1.50BSC	
Nd		1.50BSC	
E	2.90	3.00	3.10
E2	1.41	1.56	1.70
K	0.20	---	---
L	0.30	0.40	0.50
aaa		0.08	

Pin Definitions

Pin Number	functional symbol	Functional Description	Pin Number	functional symbol	Functional Description
1	GND	radio-frequency zone	9	VSS	negative supply (electricity)
2	GND	radio-frequency zone	10	VCTRL	Control Input Ports
3	RFC	RF input	11	LS	Logic Select Input Port
4	GND	radio-frequency zone	12	VDD	bias voltage (electronics)
5	GND	radio-frequency zone	13	GND	radio-frequency zone
6	GND	radio-frequency zone	14	RF1	RF output
7	RF2	RF output	15	GND	radio-frequency zone
8	GND	radio-frequency zone	16	GND	radio-frequency zone

truth table

Control and bias inputs				signaling pathway state	
Negative Supply (VSS)	Bias Voltage (VDD)	Console (LS)	Console (VCTRL)	RFC to RF1	RFC to RF2
-2V	5V	High	Low	Off	on
-2V	5V	High	High	on	Off
-2V	5V	Low	Low	on	Off
-2V	5V	Low	High	Off	on

Working Principle

1. This switch requires a supply voltage to be applied to the VDD pin. It is recommended that a capacitor be assembled on the supply line to minimize RF coupling.
2. Control is provided by two digital control voltages applied to the VCTRL pin and the LS pin. It is recommended that a small bypass capacitor be installed on these digital signal lines to improve RF signal isolation.
3. The RF input port (RFC) and RF output ports (RF1 and RF2) are internally matched with 50Ω, so no external matching is required. The RF pins are DC-coupled, and isolation capacitors are required around the RF terminals. The design is bi-directional and the inputs and outputs are interchangeable. If the external ports of the chip are connected to zero potential, no isolation capacitors are needed, otherwise isolation capacitors are required.
4. With the logic level of pin LS at High, this switch has two modes of operation: on and off. Depending on the logic level applied to the VCTRL pin, one RF output port (e.g., RF1) is set to the open mode, through which an insertion loss path is provided from the input to the output, while the other RF output port (e.g., RF2) is set to the off mode, by which the output is isolated from the input. When an RF output port (RF1 or RF2) is in isolation mode, it is internally terminated to 50Ω and the port absorbs the applied RF signal.
5. In the case that the logic level of pin LS is LOW, the control relationship is as shown in the above truth table.

Recommended power supply sequence

1. GND is energized.
2. VDD energized.
3. Turn on the digital control inputs. The relative order of the digital control inputs is not important. Turning on the digital control inputs before the VDD supply may inadvertently cause bias and damage to the ESD protection structure.
4. Turn on the RF input.

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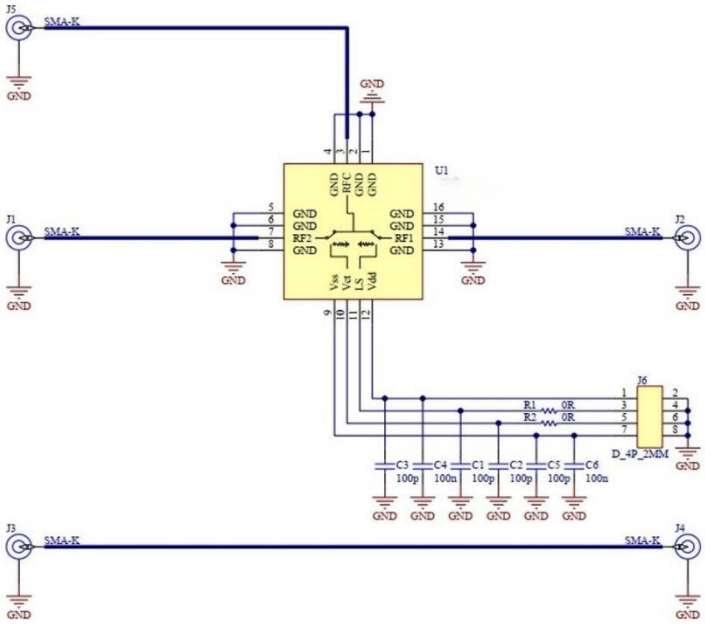
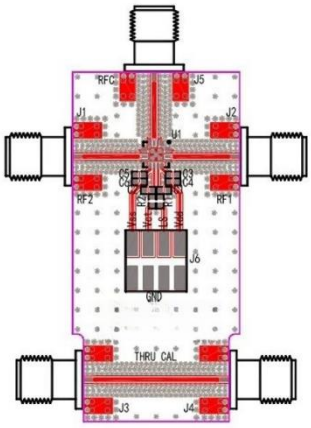
evaluation board





DeCWgnator	Description
C1, C2, C3, C5	100pF Ceramic Capacitor 0402
C4,C6	100nF Ceramic Capacitor 0402
J1, J2, J5	SMA-K PCB connectors
J6	4Pin 2mm DC Pin
R1, R2	0Ω Resistance 0402
U1	CWS110ASP3
J1,J2,J5 recommended SMA connector NJOYMAN D550B12E01-048	
NC indicates an unused port or the device is not soldered. The NC port on the chip is externally connected to GND.	

Circuit Board:Rogers4350B

The circuit board of the device application should be designed according to the design method of RF circuit, the signal line is designed according to 50Ω impedance, and the grounding pin of the package shell is close to the ground (similar to that in the figure), and there should be enough grounding holes to connect the top layer and the grounding ground of the bottom layer.