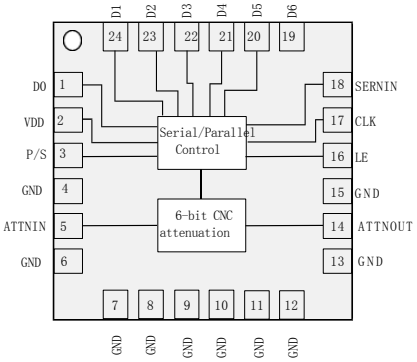
Performance Characteristics

- Operating frequency band: 0.1GHz～6GHz
- Low insertion loss: 0.5dB @0.1GHz to 2GHz (typ)
  0.9dB @2GHz to 4GHz(typ)
  1.4dB @4GHz to 6GHz(typ)
- Attenuation range: 0.5dB～31.5dB
- Package Size: 24-pin QFN, 4mmx4mm

typical application

- Mobile infrastructure
- satellite communications
- microwave
- Instrumentation

functional block diagram



summarize

The CWAT083SP4 is a six-bit numerically controlled attenuator with a frequency range of 0.1GHz to 6GHz and an insertion loss of less than 1.4dB typical. High attenuation accuracy, 0.5dB attenuation step, 3V bias voltage.

The CWAT083SP4 attenuator is available in a 24-pin, 4mmx4mm surface mount, leadless plastic package. The pin pads are coated with Sn or NiPdAu.

Electrical performance table (TA=+25℃,VDD=3.3V)

Parameter name	working conditions	minimum value	typical value	maximum values	unit (of measure)
frequency range		0.1		6	GHz
insertion loss	0.1GHz~2GHz		0.5	0.8	dB
	2GHz~4GHz		0.8	1.3	dB
	4GHz~6GHz		1.3	1.8	dB
Attenuation range	0.2GHz~6GHz	0.5		31.5	dB
Attenuation accuracy	0.2GHz~6GHz	-0.5		1	dB
Input and output return loss			20		dB
Bias Voltage (VDD)		3	3.15	3.3	V
Bias Current (IDD)				1	mA
0.1dB compression point input power (P0.1dB)			21		dBm
Input third-order intercept point			TBD		dBm
Switching time (insertion loss state to maximum attenuation state)	10% to 90% RF output		240		ns
Switching time (maximum attenuation state to insertion loss state)	10% to 90% RF output		100		ns
switching time	50% Vctl to 10%/90% RF output		300		ns
Recommended Input Power				20*	dBm

*This indicator is only the reference data for the engineering validation lot, and the indicator for the official mass production lot is 23dBm.

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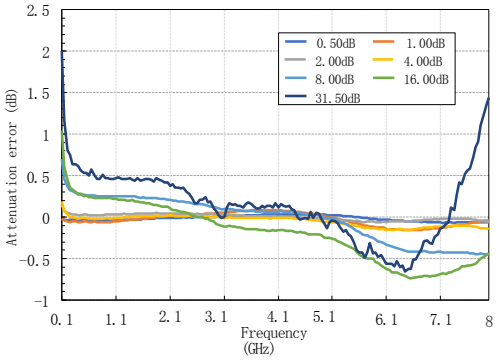
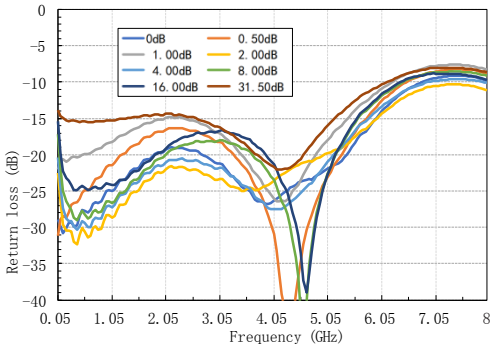
test curve

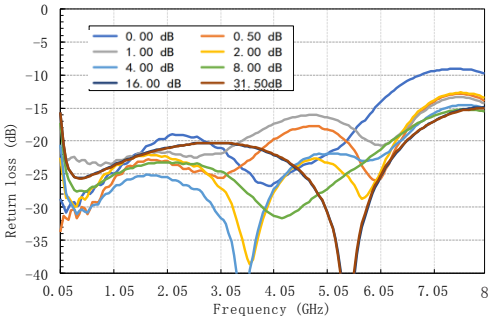
Attenuation Error VS Frequency



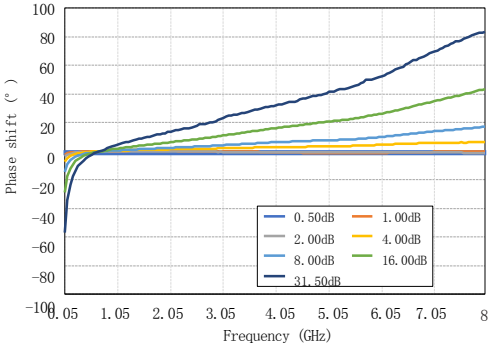
Input Return Loss VS Frequency



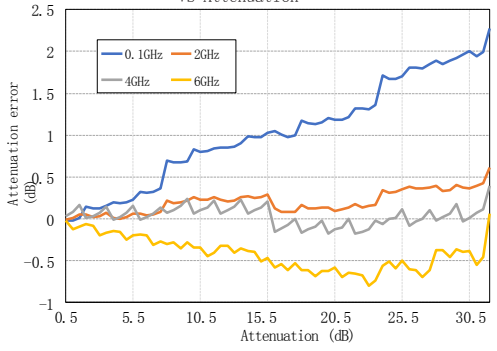
Output Return Loss VS Frequency



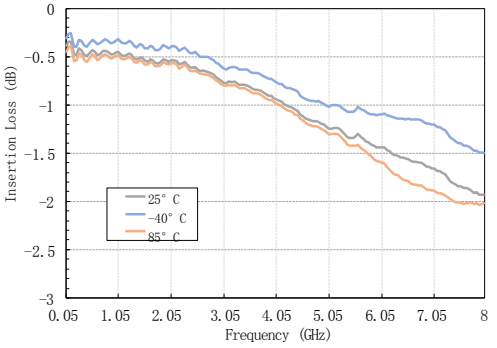
Phase Shift VS Frequency



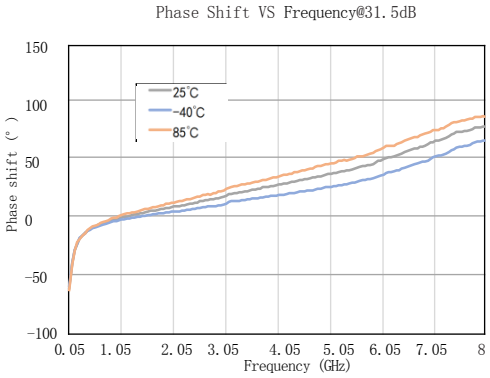
Attenuation Error
VS Attenuation



Insertion Loss VS Frequency



test curve



Operating parameters

Bias voltage VDD	3V to 3.3V
Control voltage VCTL	0V to 0.3V (Low) 3V to 3.3V (High)
operating temperature	-40℃～+85℃

Control Port: D0~D5, P/S, LE, CLK, SERNIN

Absolute maximum rating

RF Input Power	+22dBm*
Bias Voltage VDD	-0.3V~3.6V
Control Voltage VCTL	-0.5 V~VDD+0.3V
Storage temperature	-65℃～+150℃

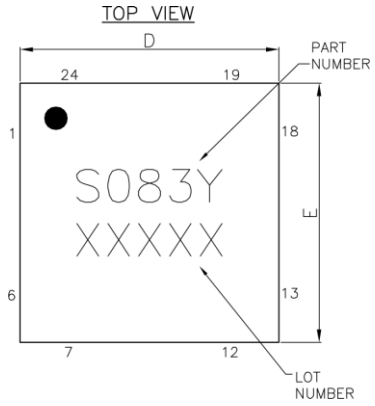
*This indicator is only the reference data for the engineering validation lot, and the indicator for the official mass production lot is 26dBm.

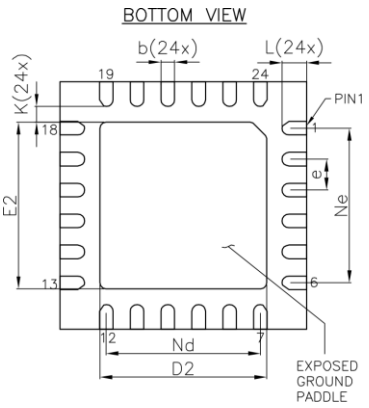
Package Information

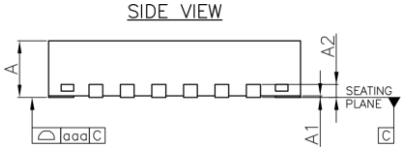
model number	package material	Pad plating	MSL rating [1]	Package identification [2]	environmental requirement
CWAT083SP4	Green resin compounds	Sn or NiPdAu	MSL 3	S083 XXXXX	RoHS compliant

[1] Maximum reflow temperature 260° C
[2] XXXXX is the lot number

Overall dimensions







Description:

1. Unit: mm
2. Lead frame material: copper alloy
3. Package surface warpage: not more than 0.05mm
4. All ground pins should be connected to PCB RF ground.

Dimension Table (unit:mm)

Symbol	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	---	0.05
A2		0.20Ref	
b	0.20	0.25	0.30
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
e		0.50BSC	
Ne		2.50BSC	
Nd		2.50BSC	
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
K	0.20	---	---
L	0.30	0.40	0.50
aaa		0.08	

Pin Definitions

Pin Number	functional symbol	Functional Description	Pin Number	functional symbol	Functional Description
1	DO	Console O port	13	GND	radio-frequency zone
2	VDD	DC Bias	14	ATTNOUT	RF Output, no isolation capacitors
3	P/S	serial-to-parallel selector terminal	15	GND	radio-frequency zone
4	GND	radio-frequency zone	16	LE	enabling terminal
5	ATTNIN	RF Input, No Barrier Capacitors	17	CLK	clock side
6	GND	radio-frequency zone	18	SERNIN	Serial Data Input
7	GND	radio-frequency zone	19	D6	let sth. lie idle
8	GND	radio-frequency zone	20	D5	Console 5 ports
9	GND	radio-frequency zone	21	D4	Console 4 ports
10	GND	radio-frequency zone	22	D3	Console 3 ports
11	GND	radio-frequency zone	23	D2	Console 2 ports
12	GND	radio-frequency zone	24	D1	Console 1 port

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truth table

Control Port Status						Attenuation status (dB)
D5	D4	D3	D2	D1	D0	
Low	Low	Low	Low	Low	Low	zero state (math.)
Low	Low	Low	Low	Low	High	0.5
Low	Low	Low	Low	High	Low	1.0
Low	Low	Low	High	Low	Low	2.0
Low	Low	High	Low	Low	Low	4.0
Low	High	Low	Low	Low	Low	8.0
High	Low	Low	Low	Low	Low	16.0
High	High	High	High	High	High	31.5

Any combination of the above states will provide attenuation approximately equal to the sum of the selected bits

Control mode selection

P/S status	control mode
Low	side by side (of two processes, developments, thoughts etc)
High	confuse two lines

The P/S pin must remain in a valid logic state (High or Low) and must not be left floating

Serial control output

The serial control interface is active when the P/S pin is set high.

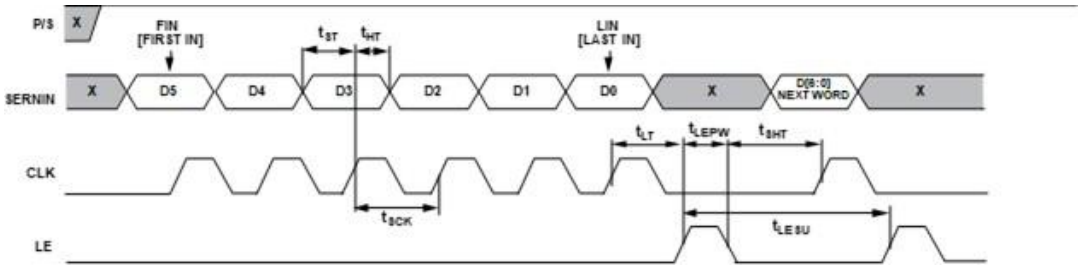
In serial mode, the six-bit serial data is first clocked to the highest bit when the CLK edge rises to the shift register, and then LE must be switched high to latch the new attenuation state. LE must be set low to write a set of six bits to the shift register, as CLK is masked to prevent the attenuation value from changing while LE remains high.

During serial mode operation, the serial control inputs (LE, CLK, SERNIN) and parallel control inputs (D0 through D5) must be maintained at valid logic levels (High or Low) at all times and must not be left floating. If the device driving these input lines experiences high impedance during sleep, it is recommended that the parallel control inputs be connected to ground and that pull-down resistors be used on all serial control input lines.

RF Input and Output

The attenuator is bi-directional; the ATTNIN and ATTNOUT pins are interchangeable as RF input and output ports. The attenuator is internally matched to 50Ω on the input and output; therefore, no external matching is required. The RF pins are DC coupled; therefore, DC blocking capacitors are required on the RF lines.

Control mode selection



Serial Control Timing Diagram

Parallel control output

The parallel control port has six digital control inputs (D5 through D0) for setting the attenuation value.D5 is the highest valid bit for selecting 16 dB attenuation and D0 is the lowest valid bit for selecting 0.5 dB attenuation.

During parallel mode operation, the serial control inputs (LE, CLK, SERNIN) and parallel control inputs (D0 through D5) must always be maintained at a valid logic level (High or Low) and must not be left floating. If the devices driving these input lines have high impedance during sleep, it is recommended that the serial control inputs be connected to ground and that pull-down resistors be used on all parallel control input lines.

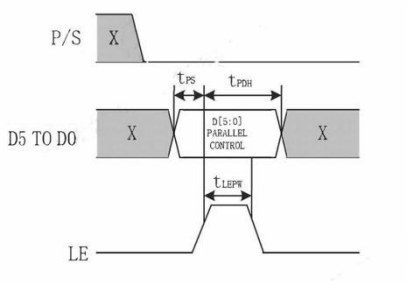
Parallel mode is enabled by setting P/S low. There are two modes of parallel operation: direct parallel mode and latching parallel mode.

Direct parallelism

For direct parallel mode, LE must be held high. The attenuation state is changed directly using the control voltage inputs (D0 through D5). This mode is ideal for manually controlling the attenuator and using hardware, switches or jumpers.

Latch Parallel Mode

When changing the control voltage inputs (D0 through D5) to set the attenuation state, the LE port must be held low. To set the desired state, LE must be switched high to transfer 7-bit data to the attenuator array bypass switch and then low to latch the change into the device.



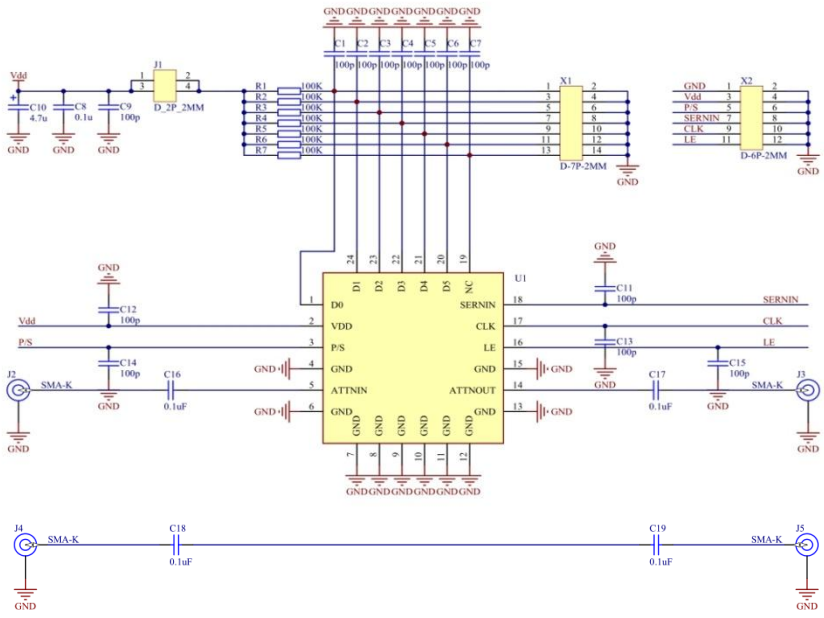
Latch Parallel Mode Timing Diagram

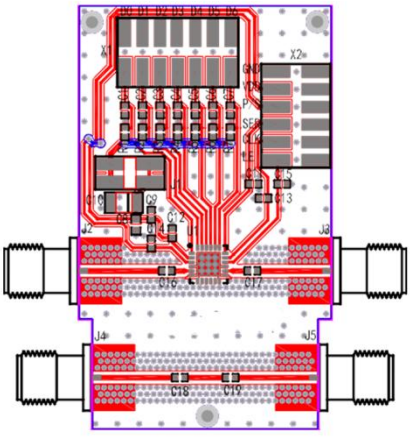
Power-up sequence and status

1. GND is energized.
2. VDD energized.
3. Turn on the digital control inputs (the relative order of the digital control inputs is not important).
4. Turn on the RF input.
5. For latched parallel mode, the LE must be switched. the relative order of the digital inputs does not matter as long as the inputs are energized after ground and VDD.

When energized, the logical state of the unit is maximum attenuation when LE is set to low. The attenuator locks at the desired energized state after approximately 200ms of energization.

evaluation board



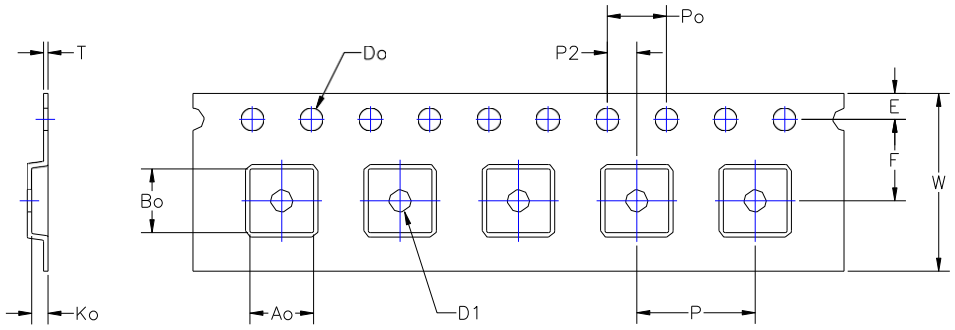


Designator	Description
c1, c2, c3, c4, c5, c6, c7, c9, c11, c12, c13, c14, c15	100pF Ceramic Capacitor 0402
C8	0.1uF Ceramic Capacitor 0603
C10	4.7uF Tantalum Capacitor 3216
C16, C17, C18, C19	0.1uF Ceramic Capacitor 0402
J1	4Pin 2mm DC Pin
J2, J3, J4, J5	SMA PCB connectors
r1, r2, r3, r4, r5, r6, r7	100k resistor 0402
U1	CWAT083SP4
X1	14Pin 2mm DC Pin
X2	12Pin 2mm DC Pin
J1, J2, J3 recommended SMA connector NJOYMAN D550B12E01-048	

Circuit Board:Rogers4350B

Device application board should be designed in accordance with the design of RF circuits, signal lines according to the 50 Ω impedance design, while the package shell of the ground pin near the ground (similar to the figure), connecting the top and bottom grounding surface should be sufficiently many grounding holes.

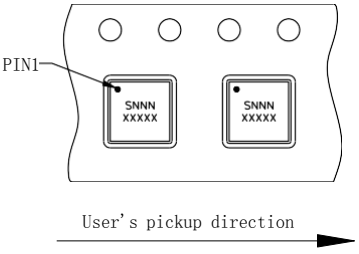
Packaging Information



DIMENSION	SPEC
W	12.00 +/-0.30
Do	Ø1.50 +0.10/-0.00
Po	4.00 +/-0.10
E	1.75 +/-0.10
D1	Ø1.50 MIN
Ao	4.30 +/-0.10
Bo	4.30 +/-0.10
P	8.00 +/-0.10
P2	2.00 +/-0.10
Ko	1.10 +/-0.10
T	0.30 +/-0.05
F	5.50 +/-0.05

Orientation of components in the carrier tape

(Tape and Reel Facing)



Description:

1. Unit: mm
2. Material: anti-static polypropylene
3. Color: black
4. 10 positioning hole center distance (P0) cumulative tolerance ± 0.2

caveat

1. Attempts to clean the chip surface with wet chemical methods are prohibited.
2. This product is a static sensitive device, storage and use of attention to anti-static.
3. Store in a dry environment.

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