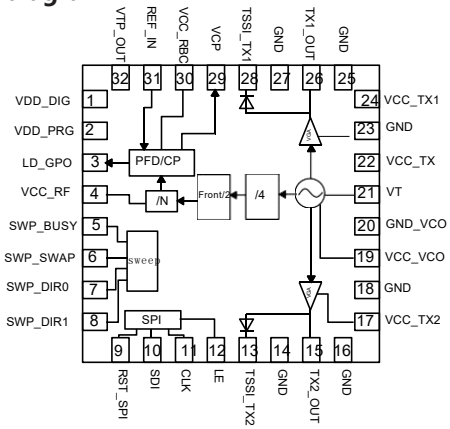
Performance Characteristics

- VCO frequency range: 23~25GHz
- VCO Low Phase Noise: -92dBc/Hz @100kHz
- Integrated fractional PLL and arbitrary waveform sweep function
- Integrated temperature and power sensing
- 3.3V power supply, low power consumption

typical application

- Satellite communication systems
- point-to-point radio
- FMCW radar

functional block diagram



summarize

The CWTR229SP4C is a phase-locked loop with integrated VCO and its operating frequency covers

The CWTR229SP4C is an integrated VCO phase-locked loop with operating frequency covering 23~25GHz, with fractional frequency divider and sweep function, supporting automatic and triggered sweep modes, realizing triangular, sawtooth, trapezoidal, and arbitrary waveform sweep waveforms, and outputting corner indication, sweeping direction, and operating status indication, including temperature and power sensors.

Electrical Performance Table (TA=+25° C VDD_PRG=5V VDD_DIG=VCC_RF=VCC_TX2=VCC_VCC=VCC_TX=VCC_TX1=VCC_BRC=3.3V)

test parameter	descriptive	unit (of measure)	Indicator parameters		
			minimum value	typical value	maximum values
REF parameters					
REF Frequency Range	Input Sine Wave	MHz		100	
Input power range		dBm	-10		10
REF Crossover Ratio			1		16383
Frequency range of phase detection	integer mode	MHz		100	
	fractional part of a number mode	MHz		100	
RF parameters					
RF Frequency Range	integer mode	GHz	23		25
N Crossover Ratio	Turn on the front 2 crossover		32		1048574
	Turn off the front 2 crossover		16		524287
Crossover ratio (decimal)	Turn on the front 2 crossover		40		1048575
Charge Pump Parameters					
Minimum CP Current		mA		TBD	
Maximum CP Current		mA		TBD	
CP leakage current		mA		TBD	

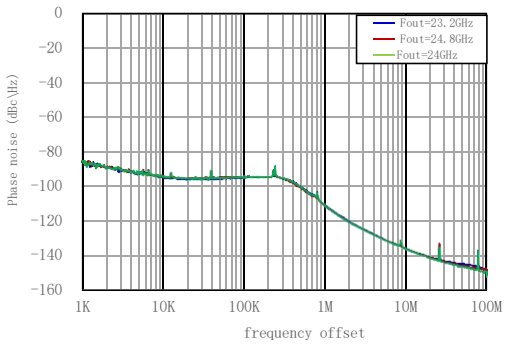
Electrical Performance Table (TA=+25° C VDD_PRG=5V VCC_RF=VCC_TX2=VCC_VCC=VCC_TX=VCC_TX1=VCC_BRC=3.3V)

test parameter		descriptive	unit (of measure)	Indicator parameters		
				minimum value	typical value	maximum values
PLL Closed Loop Parameters						
normalized background noise[e]		@ offset 100KHz, integer mode PD=100MHz, VCO=24GHz	dBc/Hz		-263	
flicker noise[e]			dBc/Hz		TBD	
phase noise	Phase noise @ 100kHz	Gain Max Fractional Mode Fout=25GHz	dBc/Hz		-82	
	Phase noise @ 1MHz		dBc/Hz		-112	
	Phase noise @ 10MHz		dBc/Hz		-137	
phase noise	Phase noise @ 100kHz	Gain maximum Integer number mode Fout=24GHz	dBc/Hz		-95	
	Phase noise @ 1MHz		dBc/Hz		-101	
	Phase noise @ 10MHz		dBc/Hz		-138	
stray	integer-boundary spuriousness		dBc/Hz		TBD	
	forensic hybridization		dBc/Hz		TBD	
Lock detection function		TBD				
VCO						
Tuning voltage (VT)			V	0		5
tuning sensitivity			GHz/V			
phase noise Fout=24GHz		@ offset 100KHz	dBc/Hz		-92	
		@ offset 1MHz	dBc/Hz		-100	
		@ offset 10MHz	dBc/Hz		TBD	
VGA						
Gain control range			dB	16		
Number of gain control bits			Bit	3		
Maximum Transmit Power			dBm		7.5	
VGA Operating Voltage			V		3.3	
power wastage						
Operating Current		VDD_DIG=VCC_RF=VCC_TX2=VCC_VCO=VCC_TX=VCC_TX1=VCC_BR C=3.3V	mA		368	

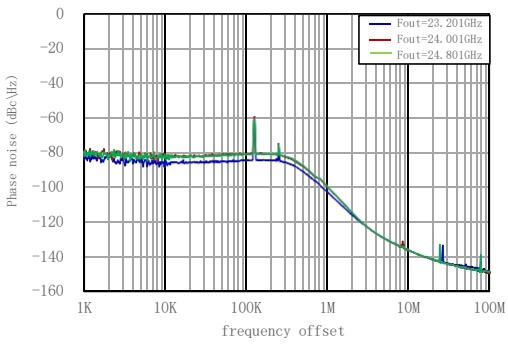
Chengdu Cuiwei Electronic Co.,LTD
Address: No. 5, Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

Test curve (VDD_PRG=5V VCC_RF=VCC_TX2=VCC_VCC=VCC_TX=VCC_TX1=VCC_BRC=3.3V)

Phase Noise VS Frequency Bias

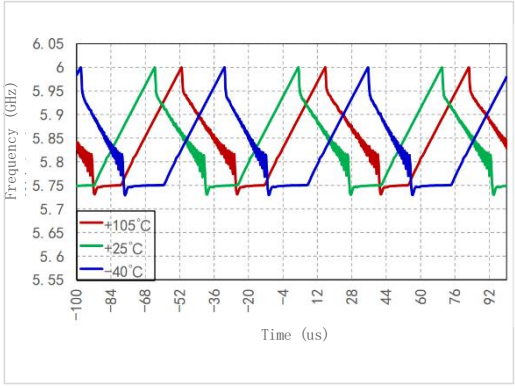


Phase Noise vs. Frequency Bias (Fout=10GHz)

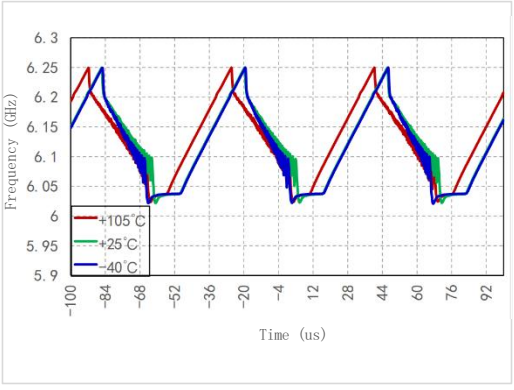


Test curve (sweep period = 66us loop bandwidth = 250KHz)

Frequency VS Time (23GHz~24GHz)



Frequency VS Time (24.15GHz~25GHz)



Temperature cycling data and temperature sensor voltage

temp	cyclicality	Temperature sensor Voltage (V)	Loss of lock in temperature patrol (observation of triangular wave and judgment by loss of lock indication signal)
-25	72us	1.852	unlatched
-15	72us	1.922	unlatched
-5	72us	1.989	unlatched
5	72us	2.057	unlatched
15	72us	2.124	unlatched
25	72us	2.189	unlatched
35	72us	2.262	unlatched
45	72us	2.333	unlatched
55	72us	2.397	unlatched

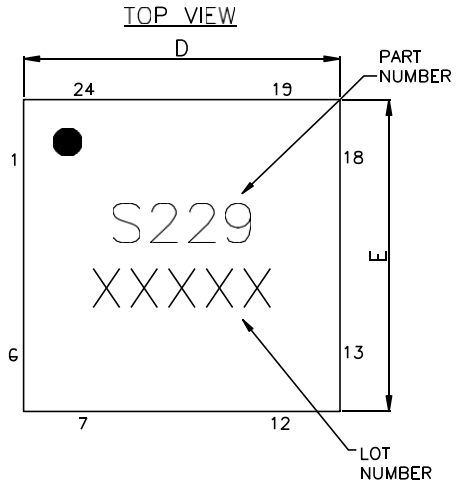
temp	Corresponds to 2000M	Temperature sensor Voltage (V)	cyclicality	Temperature Patrol Variation Loss of Lock Condition (in Sawtooth) (Wave is the object of observation)
-25	23G~25G	1.852	57us	unlatched
-15	23G~25G	1.922	57us	unlatched
-5	23G~25G	1.989	57us	unlatched
5	23G~25G	2.057	57us	unlatched
15	23G~25G	2.124	57us	unlatched
25	23G~25G	2.189	57us	unlatched
35	23G~25G	2.262	57us	unlatched
45	23G~25G	2.333	57us	lockout

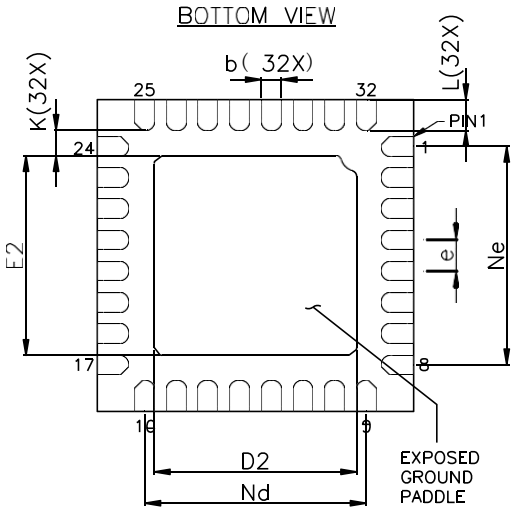
Chengdu Cuiwei Electronic Co.,LTD
Address: No. 5, Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

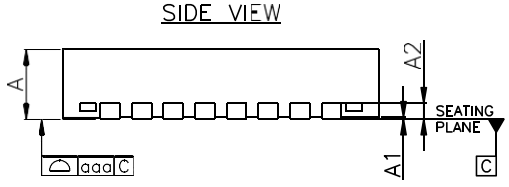
Absolute maximum rating

vdd_dig, vcc_rf, vcc_tx2, vcc_vco, vcc_tx, vcc_tx1, vcc_brc	3.6V
storage temperature	-65℃~+150℃
operating temperature	-40℃~+85℃
ESD	TBD

Package Outline Diagram







SP4C Dimension Table (unit:mm)

Symbol	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.20Ref	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
D2	2.55	2.70	2.80
e		0.40BSC	
Ne		2.80BSC	
Nd		2.80BSC	
E	3.90	4.00	4.10
E2	2.55	2.70	2.80
K	0.20	---	---
L	0.25	0.35	0.45
aaa		0.08	

Description:

1. Unit: mm
2. Lead frame material: copper alloy
3. Package surface warpage: ≤0.05mm
4. All ground pins should be connected to PCB RF ground.

Chengdu Cuiwei Electronic Co.,LTD
Address: No. 5, Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

Pin Definitions

PAD number	name (of a thing)	descriptive
1	VDD_DIG	Digital Module Power Supply, 3.3V Supply
2	VDD_PRG	OTP Power Supply, 5V Supply
3	LD_GPO	LD/GPO output port
4	VCC_RF	RF Crossover Power Supply, 3.3V Supply
5	SWP_BUSY	Sweep operation status indication
6	DIR_SWAP	Sweep direction switching indication
7	RAMP_DIR0	Sweep Direction Polarity Indication Signal Low
8	RAMP_DIR1	Sweep Direction Polarity Indication Signal High
9	RST_SPI	SPI register reset, internal integrated 80kΩ pull-down, 3.3 level
10	SDI	SPI serial data input, 3.3 level
11	CLK	SPI serial clock input, 3.3 level
12	LE	SPI serial-to-parallel conversion control signal, rising edge triggers serial data write.
13	TSSI_TX2	Transmit 2-channel power detection
14	GND	grounding port
15	TX2_OUT	Transmit 2-channel output
16	GND	grounding port
17	VCC_TX2	Transmitter Module Power Supply, 3.3V Supply
18	GND	grounding port
19	VCC_VCO	VCO power supply, 3.3V supply
20	GND_VCO	grounding port
21	VT	VCO tuning voltage input
22	VCC_TX	Transmitter Module Power Supply, 3.3V Supply
23	GND	grounding port
24	VCC_TX1	Transmitter Module Power Supply, 3.3V Supply
25	GND	grounding port
26	TX1_OUT	Transmit 1 channel output
27	GND	grounding port
28	TSSI_TX1	Transmit 1 channel power detection
29	VCP	Charge Pump Output Port
30	VCC_REF_BIAS_CP for short VCC_RBC	Phase Discriminator/Internal Bias/Charge Pump Power Supply, 3.3V Supply
31	REF_IN	Reference clock REF input port
32	VTPSEN_OUT	Temperature detection voltage output

Pin 7 RAMP_DIR0 and Pin 8 RAMP_DIR1 pins are sweep direction indication signals, whose functions are shown in the table below (0 represents a low level such as 0V, and 1 represents a high level, the (e.g. 3.3V):

RAMP_DIR0=0, RAMP_DIR1=0	uplink sweep state
RAMP_DIR0=0, RAMP_DIR1=1	downlink sweep state
RAMP_DIR0=1, RAMP_DIR1=0	parallel sweep state (physics)
RAMP_DIR0=1, RAMP_DIR1=1	unscrambled state (i.e. not in the presence of a frequency sweep)

SPIControl Description

I. Functional description

1. HMC mode and OPEN mode are supported;
2. Supports 3-wire write-only mode and 4-wire read/write mode; (SCK, LE,SDI,LD_GPO)
3. In HMC mode and OPEN mode, the register access address is 6 bits and the address range is 00h~3Fh; the register itself is 24 bits and the undefined part is treated as reserved bit;
4. Support for exception handling.

a) Read/write operation in HMC mode requires LE signal to be high all the time. If LE signal is pulled down during read/write operation, the read/write state machine enters the initial state and waits for the next read/write operation.

b) If a register with an undefined address is written, the slave ignores the operation;

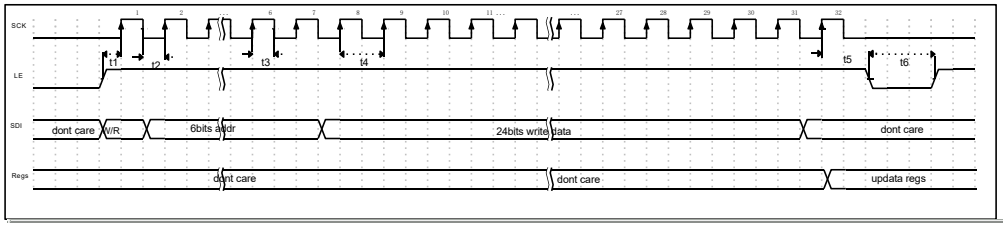
c) To read a register with an undefined address or an undefined register bit, the slave defaults to returning a register value of all zeros

II. Timing Description

hmc model

hmc mode: the rising edge of LE appears before the rising edge of SCK.

paradigm	parameters	descriptive	min	type	max	unit (of measure)
HMC	t1	LE rising edge to SCK establishment time		10		ns
	t2	SCK low level duration		10		ns
	t3	SCK high level duration		10		ns
	t4	SCK frequency		50		MHz
	t5	SCK rising edge to LE falling edge		15		ns
	t6	LE low level hold time		20		ns
OPEN	t1	SCK rising edge to LE establishment time		10		ns
	t2	SCK low level duration		10		ns
	t3	SDI Data Establishment Time		12		ns
	t4	SCK frequency		50		MHz
	t5	LE high level hold time		10		ns
	t6	SCK to LE lock data time		20		ns

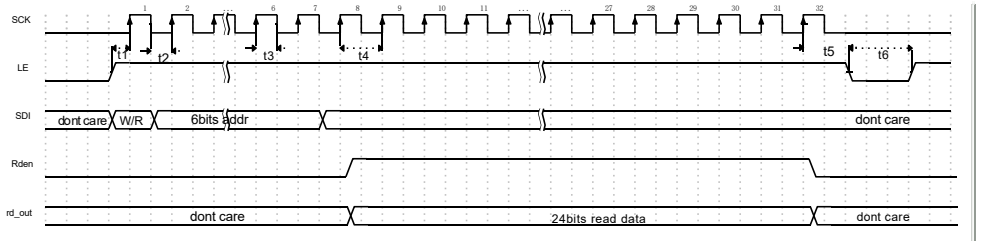


Write Status.

1: SCK first rising edge write read/write control bit; (1 SCK cycle)

2: SCK rising edge writes 6 address bits, MSB first; (2-7 SCK cycle)

3: SCK rising edge write 24-bit data, MSB priority; (8-31 SCK cycle)



Chengdu Cuiwei Electronic Co.,LTD
Address: No. 5, Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

SPI Control Description

Read state:

1: The first rising edge of SCK is written to the read/write control bit. (1 SCK cycle)

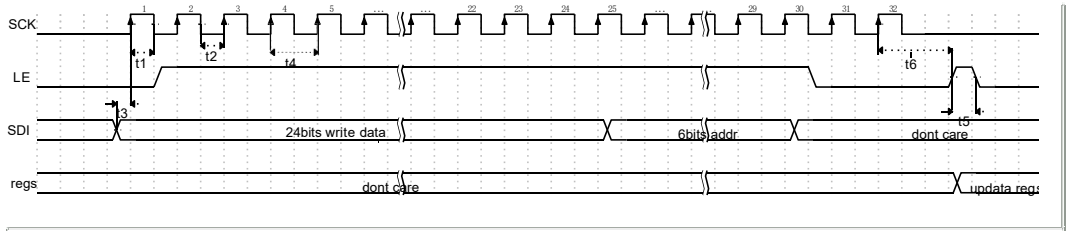
2: SCK rising edge writes 6 address bits. (2-7 SCK cycle)

3: SCK rising edge reads the value of the corresponding register (8-31 SCK cycle)

4: After a minimum delay时间t 5, the LE is cleared and a次写 cycle is completed. open mode

open mode: SCK rising edge appears before LE rising edge. open mode: 24bit data bit, 6bit address bit.

Write Status:



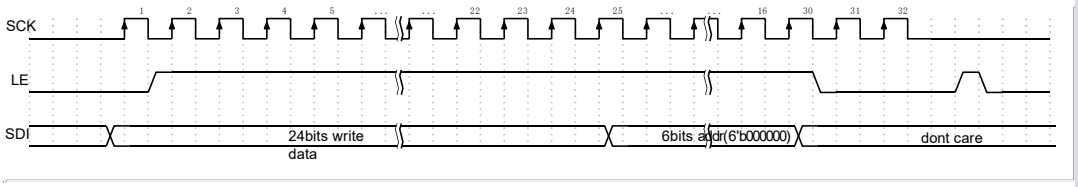
1: Write 24bit data on rising edge of SCK; (1-24 SCK cycle)

2: Write 6bit address on rising edge of SCK; (25-30 SCK cycle)

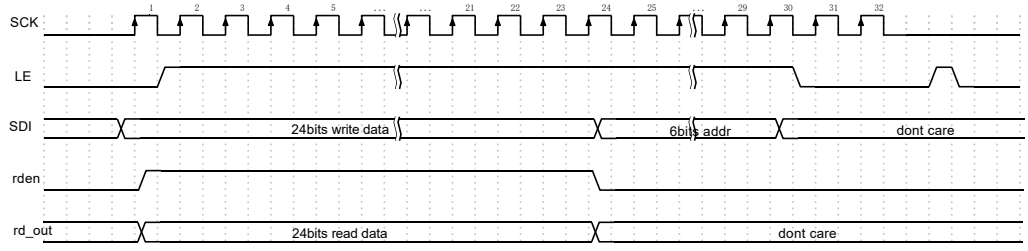
3: Set LE after the 32nd rising edge;

4: Update the corresponding register on the rising edge of LE.

Read state:



open read register 1 phase



open read register 2 phase

Phase I: Write register reg00 according to the write status of open mode; (address: 6'b000000). Phase

II: 1: LE clear. Start the second cycle of read status;

2: The address of the first cycle according to the read state (data at the address shown in register 00h[5:0]) is placed on rd_out.

SPI Control Description

III. Table of registers

name	address	christen	functionality	bit number bit	Read/ Write R/W	Default value	descriptive
Read Address Register	00	read_address	Address for SPI read data	4:0	RW	0	Use only when SPI is open mode, write the address of the register to be read, and read the data in the register corresponding to the address in SDO.
Global Shutdown Control Register	01	PD_ALL	Switch Global Control	0	RW	0	0: global normal operation 1: Global shutdown
		BLK_UVLO	Shielding of UVLO signals	1	RW	0	0: Disable undervoltage latch at power-on reset 1: Enable undervoltage lockout
Reference Frequency Divider Register	02	rdiv	Reference Crossover Ratio	13:0	RW	1	Crossover ratio 1--16383 (2^14-1)
		PD_REF	Switching Reference Crossover	14	RW	0	0: Reference crossover on 1: Turn off reference crossover, input pass-through discriminator
		RST_REF	Reset Reference Crossover	15	RW	0	Reset Reference Divider, Highly Effective
Integer frequency divider register	03	nint_dsmin	Feedback integer crossover ratio	18:0	RW	60	Valid only with swp_en=0 (non-swept mode); Off pre-division: crossover ratio 1 - 524287(2^19-1) On pre-division: crossover ratio 1 - 1048574((2^19-1) *2)
		div2	Switching pre-divider	19	RW	0	0: Turn off pre-divided frequency 1: Turn on the pre-two crossover
		PD_RF	Switching Feedback Crossover	20	RW	0	0: Feedback crossover on 1: Turn off feedback crossover
Fractional frequency divider register A	04	nfrac_dsmin	fractional crossover ratio	23:0	RW	100	Valid only if swp_en=0 (non-swept mode); set fractional crossover ratio
Default register A	05	/	/	/	/	/	/

Chengdu Cuiwei Electronic Co.,LTD
Address: No. 5, Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

SPI Control Description

III. Table of registers

name	address	christen	functionality	bit number bit	Read/Write R/W	Default value	descriptive
Fractional Frequency Control Register B	06	n_reset_dsm	reset fractional crossover frequency	0	RW	1	Initial reset signal, valid low, return to 1 after 5 phase detection cycles; 0 when power-on reset signal is valid, return to 1 after reset signal is removed.
		n_intrp	interrupt reset (computing)	1	RW	1	Interrupt reset signal, low active, reset to 1 after 5 identification cycles.
		mash_en	dsm work master mode	2	RW	1	0: dsm adopts sig-loop operation mode 1: dsm adopts mash operation mode
		fast_en	dsm working sub-mode	3	RW	0	Works with mash_en; 0: dsm adopts operating sub-mode 1 1: dsm uses working sub-mode 2
		order2_en	Order of the mash pattern	4	RW	0	Only if mash_en=1; 0: third-order mash 1: second-order mash
		int_en	Switching Integer Mode	5	RW	0	0: Fractional mode 1: Integer mode (fractional crossover disabled)
		dither_en	Jitter Mode	6	RW	0	0: LFSR jitter or no jitter (with lfsr_en) 1: Self-jittering
		lfsr_en	Switch LFSR jitter	7	RW	1	0: no jitter (only if dither_en=0) 1: LFSR jitter
		preset_en	Initial Phase Write Mode	8	RW	0	0: Initial phase internally generated 1: Initial phase external write (in conjunction with preset_phase)
		preset_trig	Initial phase rising edge Trigger	9	RW	1	Load initial phase when triggered by initial phase rising edge (internal or external write)

Chengdu Cuiwei Electronic Co.,LTD
Address: No. 5, Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

Register Description

name	address	christen	functionality	bit number bit	Read/Write R/W	default value	descriptive
fractional crossover phase register	07	preset_phase	Initial phase value	23:0	RW	100	Setting the initial phase value of the fractional crossover frequency
Sweep Control Register	08	lock_cycles	Sweep process lock cycle	15:0	RW	600	Sets the value of the sweep period from loss of lock to lock during the sweep process
		n_reset_swp	reset sweep	16	RW	1	Sweep reset signal, low active, after resetting 5 phase identification cycles Return to 1; 0 when power-on reset signal is valid, reset signal Return to 1 after removal
		swp_bypass	sweep through	17	RW	0	Valid only if swp_en=1 (swept on); equivalent to sweeping Secondary Enable for Frequency Module 0: Sweep normal output. 1: Using nint_ramp0 and nfrac_ramp1 as integers and fractional crossover ratios
		swp_trig	Trigger Signal for Sweep Trigger Mode	18	RW	0	For trigger sweep in trigger mode, rising edge active
		swp_en	Switching Sweep	19	RW	0	0: Turn off the sweep and use nint_dsmin and nfrac_dsmin as integer and fractional crossover ratio 1: Sweep on, nint_dsmin and nfrac_dsmin no efficacy
		force_lock	Latch Detect Control Sweep	23:22	RW	1	00/01: Sweep Lock Detect input controlled by Lock Detect LD exports 10: Sweep lock detection input forced to unlocked state 11: Sweep lock detection input forced to lock state

Register Description

name	address	christen	functionality	bit number bit	Read/Write R/W	default value	descriptive
Temperature Sensor and OTP Control Registers	09	TPS_OS	Temperature Sensor Output Misalignment Voltage control word	2:0	RW	0	Controls the temperature sensor's output offset voltage in steps of 3mV absolute. value, the direction of the offset is controlled by TPS_OS_DIR; 000: 3mV 001: 6mV 010: 9mV 011: 12mV 100: 15mV 101: 18mV 110: 21mV 111: 24mV
		TPS_OS_DIR	Temperature sensor output misalignment Direction control word	3	RW	0	Controls the direction of the temperature sensor output op-amp detuned voltage; 0: Positive offset for the out-of-phase voltage 1: Negative Offset of the Out-of-Sync Voltage
		TPS_TC	Temperature sensor output temperature Coefficient Slope Control Word	5:4	RW	1	Control temperature sensor output temperature slope, step size 150uV/℃, with offset direction controlled by TPS_TC_DIR; 00: 150uV/℃ 01: 300uV/℃ 10: 450uV/℃ 11: 600uV/℃
		TPS_TC_DIR	Temperature Sensor Output Temperature Coefficient Slope Direction Control Word	6	RW	0	Controls the direction of the temperature sensor output temperature slope; 0: positive slope of temperature coefficient 1: Negative slope of temperature coefficient
		PD_TPS	Switching Temperature Sensor Output Driver	7	RW	0	0: Turn on the temperature sensor 1: Turn off the temperature sensor
		OTP_CTRL	OTP control word	10:8	RW	0	OTP control word that triggers a read by default after power up; 001: Read-only 010: Pre-reading 100: burn-in other: keep it in shape
		OTP_RST	OTP Output Reset	12	RW	0	OTP output reset, rising edge triggered
		PD_OTP	Switch OTP	13	RW	0	0: Turn on OTP 1: Shutdown OTP

Register Description

name	address	christen	functionality	bit number bit	Read/Write R/W	default value	descriptive
Transceiver Control Register	10	RX1_GAIN	Receive gain control word for channel 1	2:0	RW	0	The gain control bit for receive channel 1 defaults to minimum gain in steps of about 2.85 dB; 000: 30 dB ..... 011: approximately 21.4 dB ..... 111: 10 dB
		RX2_GAIN	Receive Channel 2 gain control word	5:3	RW	0	The gain control bit for receive channel 2 defaults to minimum gain in steps of about 2.85 dB; 000: 30 dB ..... 011: approximately 21.4 dB ..... 111: 10 dB
		RX3_GAIN	Receive gain control word for channel 3	11:8	RW	0	The gain control bit for receive channel 3 defaults to minimum gain in steps of about 2.85 dB; 000: 30dB max. ..... 011: approximately 21.4 dB ..... 111: 10dB min.
		RX4_GAIN	Receive channel 4 gain control word	13:11	RW	0	The gain control bit for receive channel 4 defaults to minimum gain in steps of about 2.85 dB; 000: 30dB max. ..... 011: approximately 21.4 dB ..... 111: 10dB min.
		TX_MUTE	Switched Launch Path	14	RW	0	0: Open the launch channel 1: Close the launch channel
		TX_GAIN	Transmit Channel Gain Control Word	18:16	RW	0	Transmit channel gain control, defaults to maximum gain in steps of about 2.28 dB; 000: 16dB max. ..... 011: approximately 9.14 dB ..... 111: 0dB min.
		TX_SW	Transmit Channel Phase Control Word	20	RW	0	0: No inversion 1: Inverted phase

Chengdu Cuiwei Electronic Co.,LTD
Address: No. 5, Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

Register Description

name	address	christen	functionality	bit number bit	Read/Write R/W	default value default-dec	descriptive
Transceiver Control Register	10	TX1_MUTE	Switch Transmitter Channel 1	9	RW	0	0: Open the launch channel 1: Close the launch channel
		TX1_SW	Transmit Channel 1 Phase Control Word	10	RW	0	0: No inversion 1: Inverted phase
		TX1_GAIN	Transmit Channel 1 Gain Control Word	13:11	RW	0	Transmit channel gain control, defaults to maximum gain in steps of about 2.28 dB; 000: 16dB max. ..... 011: approximately 9.14 dB ..... 111: 0dB min.
		TX2_MUTE	Switch Transmitter Channel 2	14	RW	0	0: Open the launch channel 1: Close the launch channel
		TX2_GAIN	Transmit Channel 2 Gain Control Word	18:16	RW	0	Transmit channel gain control, defaults to maximum gain in steps of about 2.28 dB; 000: 16dB max. ..... 011: approximately 9.14 dB ..... 111: 0dB min.
		TX2_SW	Transmit Channel 2 Phase Control Word	20	RW	0	0: No inversion 1: Inverted phase

Chengdu Cuiwei Electronic Co.,LTD
Address: No. 5, Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

Register Description

name	address	christen	functionality	bit number bit	Read/Write R/W	default value	descriptive
Default Register B	11	/	/	/	/	/	/
Default register C	12	/	/	/	/	/	/
Default register D	13	/	/	/	/	/	/
Sweep integer divider output read-only registers	14	nint_swpout	Read swept integer frequency division ratio	18:0	R	/	Sweeper integer divider output, 19 bits; when swp_en=0, directly read out the integer divider value of DSM, i.e. 03d<18:0>
		swp_busy	Read sweep status	19	R	/	Sweep status indication; 0: Indicates non-sweep state 1: Indicates that the frequency is always swept
Sweep integer divider output read-only registers	15	nfrac_swpout	Read swept integer frequency division ratio	23:0	R	/	Sweeper fractional crossover output, 24 bits; with swp_en=0, the fractional crossover value of the DSM is read directly, i.e., 04d<23:0>

Register Description

name	address	christen	functionality	bit number bit	Read/Write R/W	default value	descriptive
Latch Detect and Total Parallel Output Registers	16	LD_window	Digital LD Determination Window Size	2:0	RW	0	The number LD determines the window size: 000: 2ns; 001: 5.5ns; 010: 11ns; 011: 21ns 100: ″30ns; 101: 58ns; 110: 114ns; 111: 224ns
		LD_wincnt	Digital LD window judgment Count value	4:3	RW	0	LD judgment is valid after the number of times the PFD is in the window reaches this set value: 00:64 01: 256 10:1024 11:4096
		LD_MODE	LD operating mode	5	RW	0	LD operating mode: 0: Digital LD mode (PFD delay window mode) 1: Analog LD mode (PFD duty cycle mode)
		PD_LD	Switch Latch Detection LD	6	RW	0	0: Turn on LD 1: Shutdown LD
		LD_DCC	Analog LD Duty Cycle Determination Range	10:8	RW	0	LD Duty Cycle Judgment Range: 000:10% 001: 15% 010: 20% 011: 25% 100: 30% 101: 35% 110: 40% 111: 45%
		GPO	Global parallel port output	19:16	RW	0	Analog output selection for LD_GPO_OUT pin output: 0000: NC not connected 0001: Reference divider REF_DIV 0010: Feedback divider RF_DIV 0011: Charge pump UP 0100: Charge pump DN 0101: Tuning voltage VCP_mir1 0110: Tuning voltage VCP_mir2 0111: Undervoltage lockout VUVLO 1000--1111: NC not connected Supplement: The output of LD_GPO_OUT pin is controlled by RD_EN and GPO_EN, RD_EN is always high, and RD_EN is low when there is a step (low-to-high or high-to-low) of LE (SEN). RD_EN is always high: When RD_EN=1 (high), LD_GPO_OUT=SDO (independent of whether GPO_EN is high or low); When RD_EN=0 (low) and GPO_EN=0, LD_GPO_OUT=LD; When RD_EN=0 (low) and GPO_EN=1, LD_GPO_OUT=analog output (see above)
		GPO_EN	Switch GPO	23	RW	0	0: Turn off GPO in LD mode 1: Shutdown LD with GPO mode

Register Description

name	address	christen	functionality	bit number bit	Read/Write R/W	default value	descriptive
Discriminator and Charge Pump Register A	17	PD_tdelay	Setting the PFD reset delay	1:0	RW	0	PFD reset delay: 00: 0.6ns 01: 1ns 10: 1.4ns 11: 1.8ns
		POL_INV	Setting PFD polarity	2	RW	1	PFD polarity control: 0: positive polarity 1: Reverse polarity
		PD_PFD	Switching frequency and phase discriminator PFD	4	RW	0	0: Turn on PFD 1: Turn off PFD
		FUP_CP	Forces the UP output of the PFD to be enabled.	5	RW	0	Effective only with PFD off 0: Force the UP output of the PFD to be turned off 1: Force the UP output of the PFD to be enabled
		FDN_CP	Forces the DN output of the PFD to be enabled.	6	RW	0	Effective only with PFD off 0: Forced shutdown of the DN output of the PFD 1: Forces the DN output of the PFD to be enabled
		CPGup	CP Gain Current UP Control Word	15:8	RW	255	CP gain current UP control word (20uA/bit): Current calculation: 20uA*CPGup CPGup range: 0--255
		CPGdn	CP Gain Current DN Control Word	23:16	RW	255	CP gain current DN control word (20uA/bit): Current calculation: 20uA*CPGdn CPGdn range: 0--255
Discriminator and Charge Pump Register B	18	CPOS_current	CP Compensation Current Control Word	6:0	RW	0	CP compensation current DN control word (5uA/bit): Current calculation: 5uA*CPGdn CPOS_current range: 0--127
		PD_CP	Switching Charge Pump CP	7	RW	0	0: Turn on CP 1: Shutdown CP
		CPOS_UP_EN	UP compensation current for switching CP	8	RW	0	0: Turn on the UP compensation current of the CP 1: UP compensation current for turning off the CP
		CPOS_DN_EN	DN compensation current for switching CP	9	RW	0	0: DN compensation current with CP turned on 1: Turn off the DN compensation current of the CP
		PD_BIAS	Switch bias current BIAS	10	RW	0	0: Turn on BIAS current 1: Turn off BIAS current

Chengdu Cuiwei Electronic Co.,LTD
Address: No. 5, Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

Register Description

name	address	christen	functionality	bit number bit	Read/Write R/W	default value	descriptive
Sweep control register A	19	inst_lock_en	Fast lockout for switching sweep applications	0	RW	0	0: Close Quick Lock 1: Enable Quick Lock
		chirp_delay_en	Switching Sawtooth Wave Interval	1	RW	0	Interval between two sawtooth waves in unidirectional sweep mode enable; 0: No spacing allowed 1: Interval allowed (must set inst_lock_en=0)
		swp_fast_en	Switching Fast Sweep Function	2	RW	0	Fast sweep mode enable; 0: Normal sweep 1: Fast sweep
		ramp_seg_num	Sets the number of frequency bands to be swept in any sweep mode.	6:4	RW	0	In Arbitrary Waveform mode, set the number of custom segments to be added. 000: 1 paragraph; 001: 2 paragraphs; 010: 3 paragraphs; 011: 4 paragraphs 100: 5 paragraphs; 101: 6 paragraphs; 110: 7 paragraphs; 111: 8 paragraphs
		ramp_dir	Read sweep direction status	9:8	R	/	Sweep polarity indication signal (non-sweep mode, default 0): 00: Sweep uplink 01: Sweep frequency downward 10: Sweep wait (i.e., parallel) 11: Non-sweep state
		dir_swap_flag	Read Sweep Direction Change Indication	10	R	/	Sweep corner status indication output, toggle between 0/1 Proof direction Change

Chengdu Cuiwei Electronic Co.,LTD
Address: No. 5, Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

Register Description

name	address	christen	functionality	bit number bit	Read/Write R/W	default value	descriptive
Sweep control register B	20	nint_ramp0	Setting the start of the 1st sweep Integer crossover ratio	18:0	RW	80	Sets 1st sweep start integer crossover ratio, 19 bits
		swp_fast_factor	Setting the Fast Sweep Multiplier	23:19	RW	15	The multiplier setting for the fast sweep is valid only if swp_fast_en=1; 00000: 1x speed ..... 11111: 32x speed
Sweep control register C	21	nfrac_ramp0	Setting the start of the 1st sweep Fractional crossover ratio	23:0	RW	200	Sets the starting fractional crossover ratio of the 1st sweep, 24 bits
Sweep control register D	22	step_ramp0	Setting the 1st sweep step	23:0	RW	150	Set 1st sweep step, 24 bits; Calculate step Nstep=Tramp*fref Calculate the sweep step Step=(Ntrm-Nstr)/Nstep Converted to step_swp=Step*2^24; If start divider ratio = end divider ratio, then swp_step is used as a wait clock
Sweep control register E	23	nint_ramp1	Set 1st sweep termination Integer crossover ratio	18:0	RW	80	The terminating integer frequency division ratio of segment 1 is also the starting integer frequency division ratio of segment 2
		next_mode0	Setting the segment selection trigger for paragraph 1	19	RW	0	Paragraph 1 paragraph selects the triggering method: 0: Continuous mode 1: Trigger mode
Sweep control register F	24	nfrac_ramp1	Setting 1st sweep termination Fractional crossover ratio	23:0	RW	200	The terminating fractional frequency division ratio of segment 1 is also the starting fractional frequency division ratio of segment 2, 24-bit.
Sweep control register G	25	step_ramp1	Setting the 2nd sweep step	23:0	RW	150	Set 2nd sweep step, 24 bits; Calculate step Nstep=Tramp*fref Calculate the sweep step Step=(Ntrm-Nstr)/Nstep Converted to step_swp=Step*2^24; If start divider ratio = end divider ratio, then swp_step is used as a wait clock

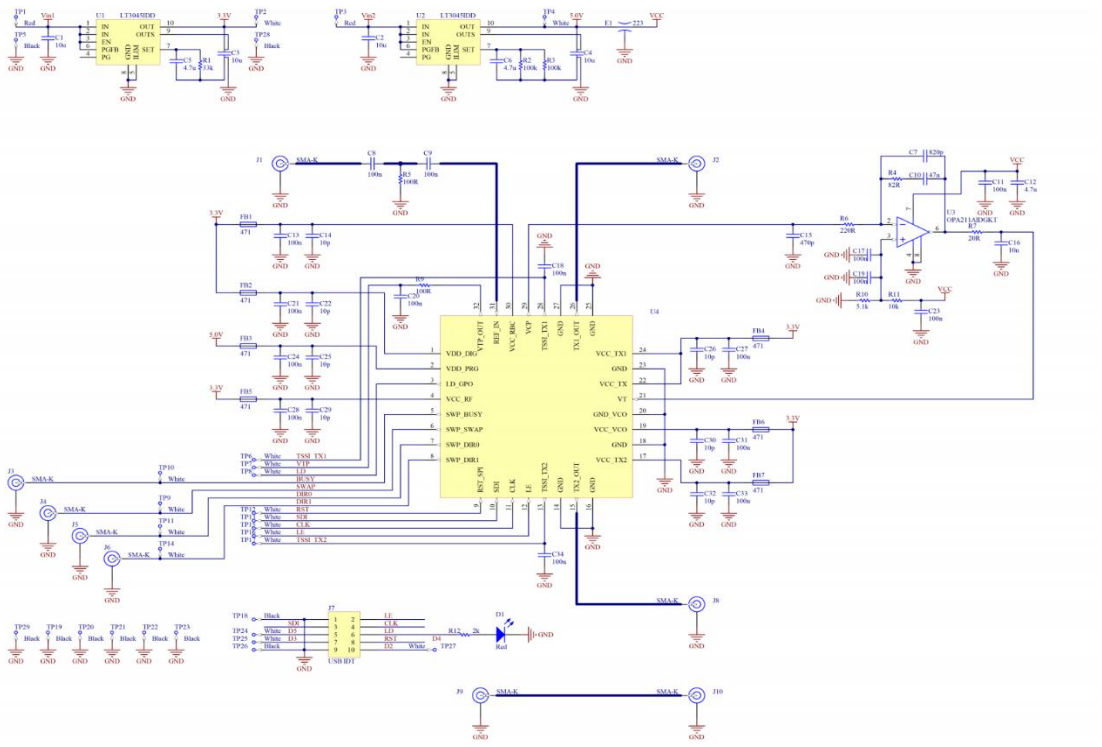
Register Description

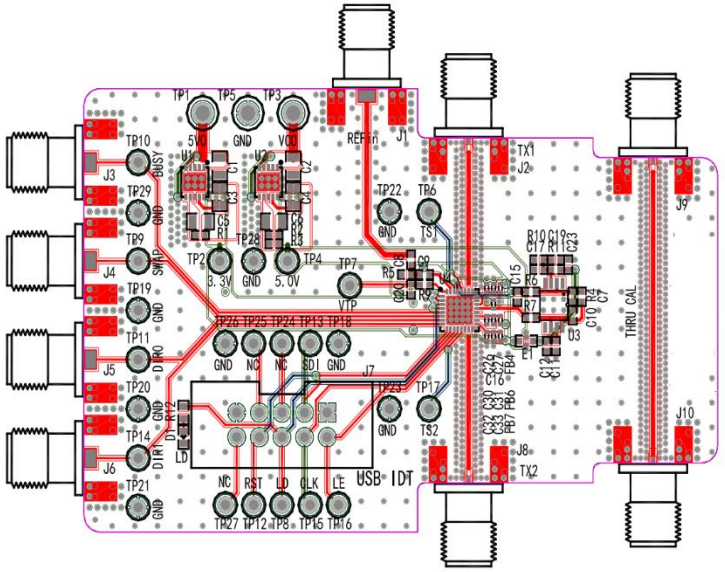
name	address	christen	functionality	bit number bit	Read/Write R/W	default value default-dec	descriptive
Sweep control register H	26	nint_ramp 2	Setting 2nd sweep termination Integer crossover ratio	18:0	RW	80	The terminating integer frequency division ratio of segment 2 is also the starting integer frequency division ratio of segment 3
		next_mode 1		19	RW	0	Paragraph 2 paragraph selects the triggering method: 0: Continuous mode 1: Trigger mode
Sweep control register I	27	nfrac_ramp 2	Setting 2nd sweep termination Decimal crossover ratio	23:0	RW	200	The terminating fractional frequency division ratio of segment 2 is also the starting fractional frequency division ratio of segment 3, 24-bit
Sweep control register J	28	step_ramp 2	Setting up the segment selection trigger for paragraph 2 Setting the 3rd sweep step	23:0	RW	150	Set the 3rd sweep step, 24 bits; Calculate step Nstep=Tramp*fref Calculate the sweep step Step=(Ntrm-Nstr)/Nstep Converted to step_swp=Step*2^24; If start divider ratio = end divider ratio, then swp step is used as a wait clock
Sweep control register K	29	nint_ramp 3	Setting 3rd sweep termination Integer crossover ratio	18:0	RW	80	The terminating integer frequency division ratio of segment 3 is also the starting integer frequency division ratio of segment 4
		next_mode 2	Setting the trigger mode for paragraph 3 segment selection	19	RW	0	Paragraph 3 paragraph selection of triggers: 0: Continuous mode 1: Trigger mode

Register Description

name	address	christen	functionality	bit number bit	Read/Write R/W	default value default-dec	descriptive
Sweep control register L	30	nfrac_ramp 3	Setting 3rd sweep termination Decimal crossover ratio	23:0	RW	200	The terminating fractional frequency division ratio of segment 3 is also the starting fractional frequency division ratio of segment 4, 24-bit
Sweep control register M	31	step_ramp 3	Setting the 4th sweep step	23:0	RW	150	Sets the 4th sweep step, 24 bits; calculates step Nstep=Tramp*fref Calculate the sweep step Step=(Ntrm-Nstr)/Nstep Converted to step_swp=Step*2^24; If start divider ratio = end divider ratio, then swp_step is used as a wait clock
Sweep control register N	32	nint_ramp 4	Setting 4th sweep termination Integer crossover ratio	18:0	RW	80	The terminating integer frequency division ratio of segment 4 is also the starting integer frequency division ratio of segment 5
		next_mode 3	Setting the trigger mode for paragraph 4 segment selection	19	RW	0	Paragraph 4 paragraph selects the trigger mode: 0: Continuous mode 1: Trigger mode

Evaluation Board Circuit Diagram





Chengdu Cuiwei Electronic Co.,LTD
Address: No. 5, Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

Evaluation Board Circuitry

#	Designator	Comment	Description	Footprint	Manufacturer	Part Number	SOB	Quantity
1	!PCB1	PCB	Printed Circuit Board		Si_Core	EVAL-SITR4SP4C-B	Y	1
2	C1, C2, C3, C4	10u	Capacitor	0805, 0805_4	TDK	C2012X5R1E106K125AB	Y	4
3	C5, C6	4.7u	Capacitor	0805	TDK	C2012X5R1E475K125AB	Y	2
4	C7	820p	Capacitor	0402	Murata	GCM1555C1H821JA16D	Y	1
5	C8, C9, C11, C13, C17, C18, C19, C20, C21, C23, C24, C27, C28, C31, C33, C34	100n	Capacitor	0402, 0402_I	Murata	GRM155R71H104KE14D	Y	16
6	C10	47n	Capacitor	0402	Murata	GRM155R71E473JA88D	Y	1
7	C12	4.7u	Capacitor	0402	TDK	C1005X5R1A475K050BC	Y	1
8	C14, C22, C25, C26, C29, C30, C32	10p	Capacitor	0402_I	Murata	GRM1555C1H100FA01D	Y	7
9	C15	470p	Capacitor	0402	Murata	GCM1555C1H471JA16D	Y	1
10	C16	10n	Capacitor	0402_I	Murata	GRM155R71H103JA88D	Y	1
11	D1	Red	LED	0603D	WE	150060SS75003	Y	1
12	E1	223	EMI Filter	NFM18C	Murata	NFM18CC223R1C3	Y	1
13	FB1, FB2, FB4, FB5, FB6, FB7	471	Resistor	0402_I	Yageo	BLM15BD471SH1	Y	6
14	FB3	471	Resistor	0402_I	Yageo	BLM15BD471SH1	N	1
15	J1, J2, J3, J4, J5, J6, J8, J9, J10	SMA-K	RF Connecter	SMA_40G, SMA_DC	傲文	D550B12E01-023	Y	9
16	J7	USB IDT	Header, 5-Pin, Dual row	IDC2.54-10		DC3-10P	Y	1
17	R1	33k	Resistor	0402	Yageo	RC0402FR-0733KL	Y	1
18	R2, R3	100k	Resistor	0402	Yageo	RC0402FR-07100KL	Y	2
19	R4	82R	Resistor	0402	Yageo	RC0402FR-0782RL	Y	1
20	R5, R9	100R	Resistor	0402	Yageo	RC0402FR-07100RL	Y	2
21	R6	220R	Resistor	0402	Yageo	RC0402FR-07220RL	Y	1
22	R7	20R	Resistor	0402	Yageo	RC0402FR-0720RL	Y	1
23	R10	5.1k	Resistor	0402	Yageo	RC0402FR-075K1L	Y	1
24	R11	10k	Resistor	0402	Yageo	RC0402FR-0710KL	Y	1
25	R12	2k	Resistor	0603	Yageo	RC0603FR-072KL	Y	1
26	TP1, TP3	Red	Test Point	Keystone5005	Keystone	Keystone5005	Y	2
27	TP2, TP4	White	Test Point	Keystone5002	Keystone	Keystone5002	N	2
28	TP5	Black	Test Point	Keystone5006	Keystone	Keystone5006	Y	1
29	TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP24, TP25, TP27	White	Test Point	Keystone5002	Keystone	Keystone5002	Y	15
30	TP18, TP19, TP20, TP21, TP22, TP23, TP26, TP28, TP29	Black	Test Point	Keystone5001	Keystone	Keystone5001	Y	9
31	U1, U2	LT3045IDD	LDO	DFN10	ADI	LT3045IDD	Y	2
32	U3	OPA211AIDGKT	Operational Amplifier	MSOP8	TI	OPA211AIDGKR	Y	1
33	U4	SITR229SP4C		SP4C	Si_Core	SITR229SP4C	Y	1

PCB tiered construction
Top Copprer 1.5oz thick
RO4350B (Er = 3.66) 10mil thick
Mid1 Copprer 1oz thick
FR-4 (Er = 4.6) 5.9mil thick
Mid2 Copprer 1oz thick
FR-4 (Er = 4.6) 25mil thick
Mid3 Copprer 1oz thick
FR-4 (Er = 4.6) 5.9mil thick
Mid4 Copprer 1oz thick
FR-4 (Er = 4.6) 10mil thick
Bottom Copprer 1.5oz thick