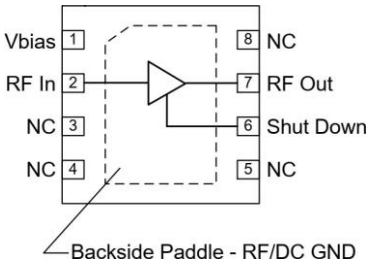
Performance characteristics

- Frequency range: 0.6 ~ 6GHz
- Ultralow noise: 0.6 dB typical
- Gain: 22.5 dB
- Output P1dB: 19.5 dBm
- Output IP3: 37dBm

Typical application

- DAS
- Mobile infrastructure
- Wireless communication
- TDD or FDD system

Functional block diagram



Overview

The CWA283SP2B is a 0.6 ~ 6GHz high performance low noise wideband amplifier manufactured using the GaAs process. The low noise amplifier can provide very low noise figure and high OIP3 in all operating frequency bands, which is very suitable for low noise and high linearity systems. At 2.6 GHz, the amplifier typically provides 23.5 dB gain, +37.5 dB OIP3, and 0.6 dB noise figure at 65 mA current. At the same time, the low noise amplifier integrates the turn-off function, which can be applied in TDD system.

It is available in a 2 x 2 mm small surface QFN package.

Electrical performance table (TA=+25 ℃, VDD=5V, IDD=65mA)

Parameter name	Describe	Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	Unit
Operating frequency	Ferq	0.6 ~ 4.2			4.2 ~ 6			GHz
Gain	S21		23.5			19.5		dB
Input return loss	S11		-12			-9.5		dB
Output return loss	S22		-12			-13		dB
Reverse isolation	S12		-28			-28		dB
Output power 1dB compression point	P1dB		20.5			18		dBm
Output IP3	Pout = +5 dBm/tone, Δf = 1 MHz		36.5			35.5		dBm
Saturated power	P3dB		21.5			20.5		dBm
Noise figure	NF		0.6			0.7		dB
On/off state control voltage (pin 6)	Open state	0		0.63	0		0.63	V
	Off state	1.17		5	1.17		5	V
Current (IDD)	Open state		65			65		mA
	Off state		4			4		mA
Switching time	LNA ON to OFF		50			50		nS
	LNA OFF to ON		50			50		nS

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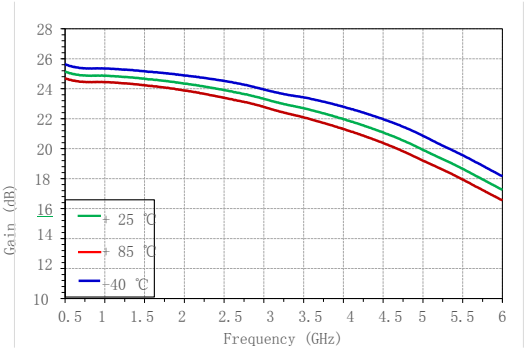
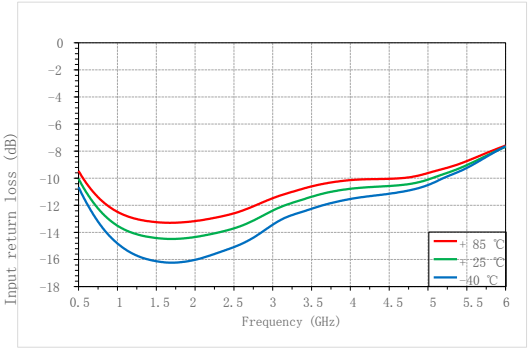
Test curve

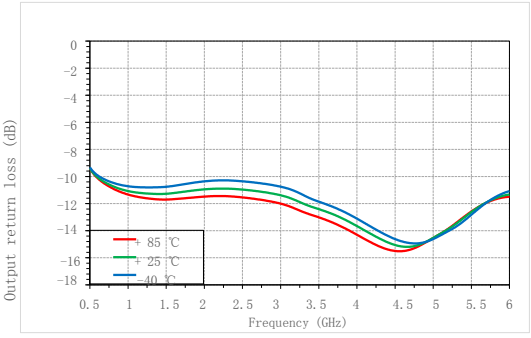
Gain VS frequency



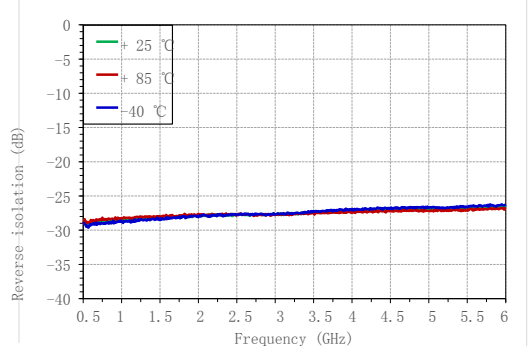
Input return loss VS frequency



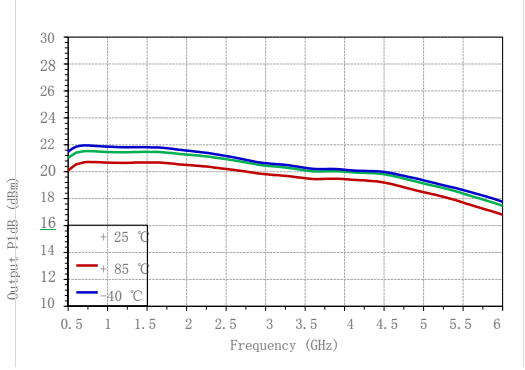
Output return loss VS frequency



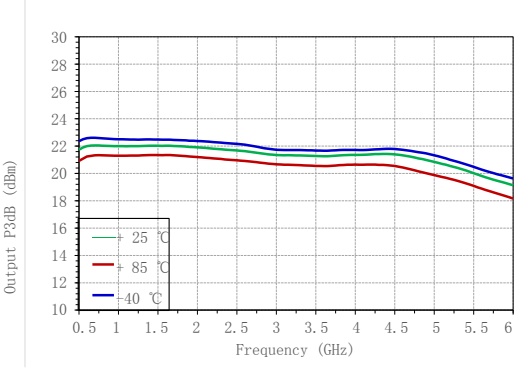
Reverse isolation VS frequency



Output P1dB VS frequency



Output P3dB VS frequency



CWA

Amplifier series

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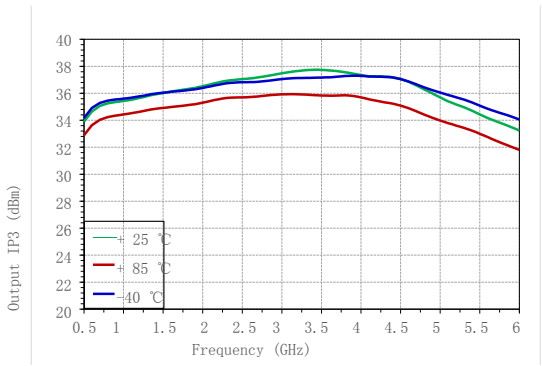
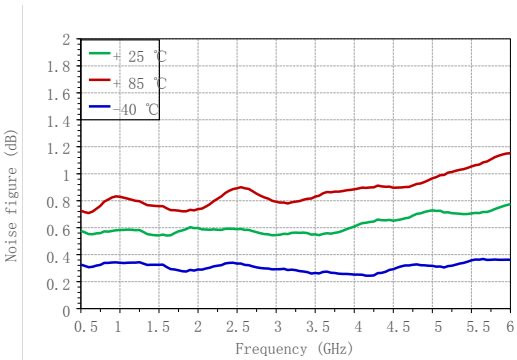
Test curve

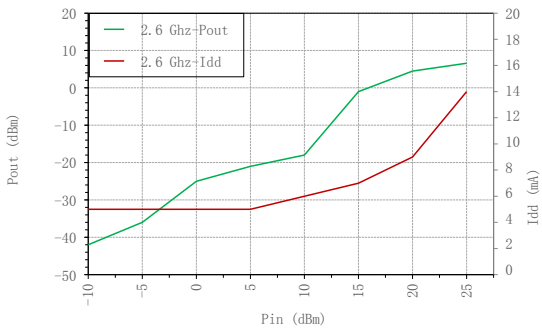
Output IP3 VS frequency



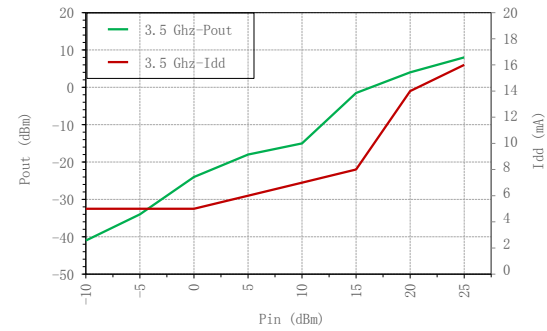
Noise figure VS frequency



Shutdown state Pout & Idd VS Pin
(Ferq=2. 6GHz)



Shutdown state Pout & Idd VS Pin
(Ferq=3. 5GHz)



Recommended operating parameters

Indicators	Minimum value	Typical value	Maximum value
Operating temperature (℃)	-40		85
Bias voltage VDD (V)	3.3	5	5.25

Absolute maximum rating

Storage temperature	-65 ℃ ~ + 150 ℃
Bias voltage VDD	7V
Input power, CW, 50 Ω, T = 25 ° C	+ 22dBm
Input power, CW, shutdown state	+ 25dBm
ESD-HBM	TBD

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Encapsulation information

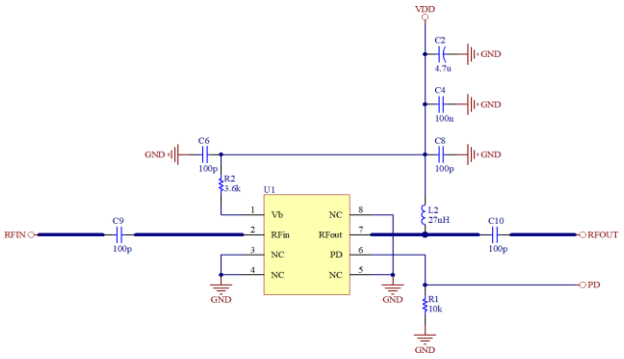
Model	Packaging material	Pad coating	MSL Rank [1]	Package ID [2]	Environmental protection requirements
CWA283SP2B	Green resin compound	NiPdAu	MSL 3	S283 XXXX	RoHS compliant

[1] Maximum reflow soldering temperature 260 ℃
[2] XXXXX is the batch number

Typical properties (TA=+25 ℃, VDD=5V, IDD=65mA)

Indicators	Unit						
Frequency	GHz	0.9	1.9	2.6	3.5	4.2	4.8
Gain	dB	24.8	24.4	23.8	22.7	21.6	20.4
Input return loss	dB	-13	-14.4	-13.5	-11.4	-10.7	-10.4
Output return loss	dB	-10.9	-11	-11	-12.4	-14.2	-15.1
Noise	dB	0.5	0.6	0.6	0.5	0.7	0.7
Output power 1dB compression point	dBm	21.4	21.3	20.8	20	19.9	19.4

Typical application diagram



DeCWgnator	Description
C2	4.7 uF
C4	100nF
C6, C8, C9, C10	100pF
L2	27nH
R3	0 Ω
R2	3.6 k Ω
R1	10k Ω

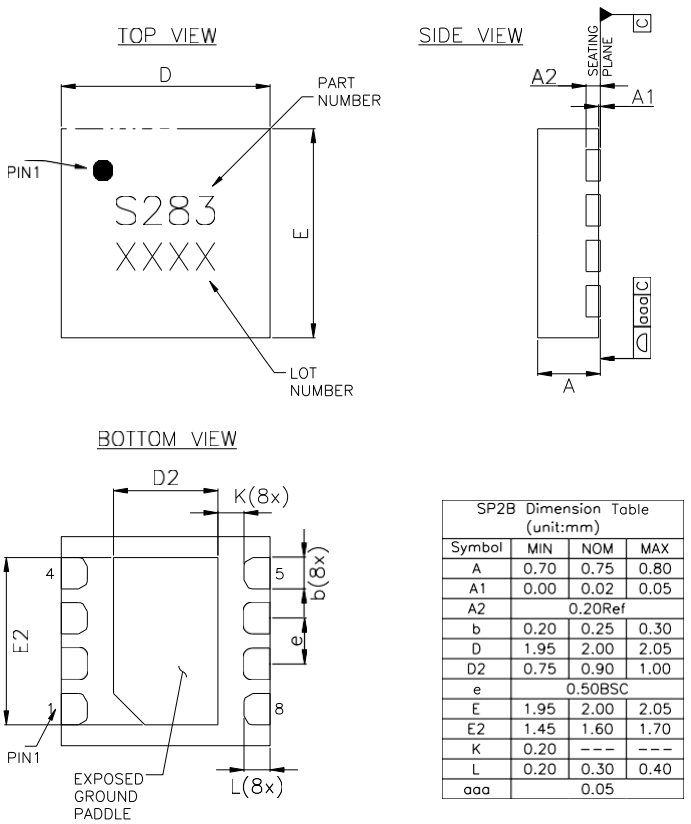
Note:

1. For FDD applications, R1 = 10 K Ω or connect pin 6 to GND. At the same time, R3 does not weld the device.
2. For TDD applications, R1=10K and R3=0 Ω.
3. R2 is used to set the current, and different current values mainly affect the performance of OIP3 and P1dB. Typical value: 3.6 K Ω-65mA @ 5V

Pin definition

Pin No.	Label	Description
1	Vbias	The bias voltage pin can change the static operating point of the chip by adjusting the resistance value of R2
2	RF In	RF input, no DC blocking capacitor inside the chip
6	Shut Down	The chip is turned off when the pin is at high voltage (> 1.17 V); The pin is grounded or the driving voltage is lower than 0.63 V, Then the chip is in an open state and works normally.
7	RF Out/DCBias	RF output pin, there is no DC blocking capacitor inside the chip. DC bias voltage also needs to be supplied to chip and core through this pin There is no bias inductor inside the chip.
3, 4, 5, 8	NC	No connection or grounding is required
Backside Paddle	RF/DC GND	RF/DC grounding.

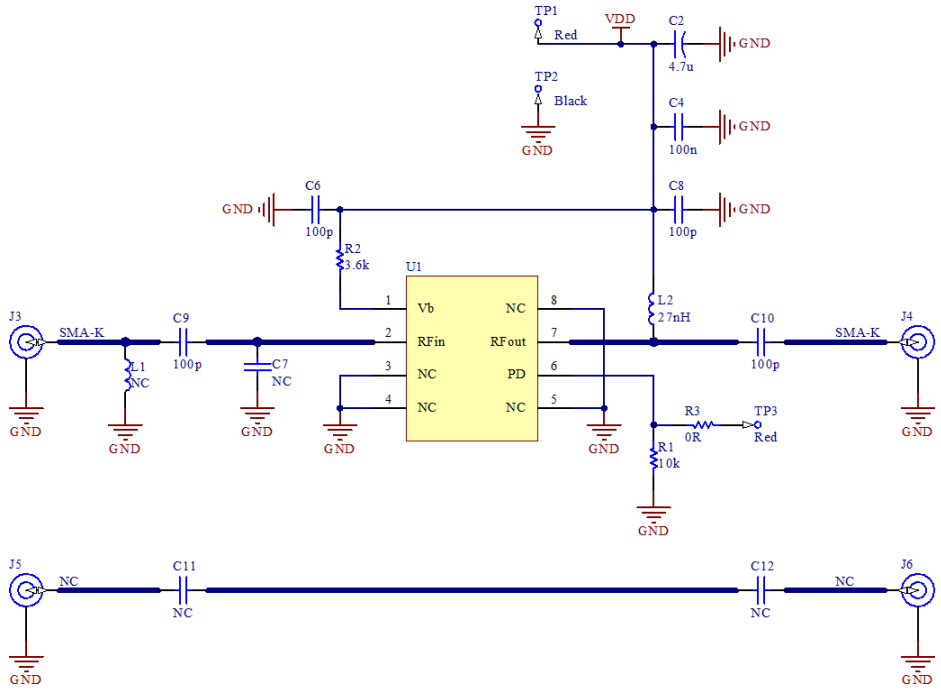
Package outline drawing

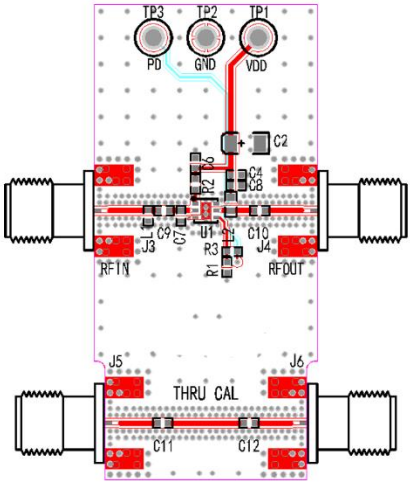


SP2B Dimension Table (unit:mm)

Symbol	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.20Ref	
b	0.20	0.25	0.30
D	1.95	2.00	2.05
D2	0.75	0.90	1.00
e		0.50BSC	
E	1.95	2.00	2.05
E2	1.45	1.60	1.70
K	0.20	---	---
L	0.20	0.30	0.40
aaa		0.05	

Evaluation board circuit diagram





DeCWgnator	Description
C2	Tantalum capacitor 1206 4.7 uF
C4	Multilayer Ceramic Capacitor 0402 100nF
C6, C8, C9, C10	Multilayer Ceramic Capacitor 0402 100pF
L2	Wound inductor 0603 27nH
R3	Resistance 0402 0 Ω
R2	Resistance 0402 3.6 k Ω
R1	Resistance 0402 10k Ω
J3, J4	SMA-K PCB Connector
TP1, TP2, TP3	DC Test Terminal
U1	CWA283SP2B
Nanjing Aowen D550B12E01-023 SMA-K connector is recommended for J3 and J4	
NC means that ports are not used or the device is not soldered. The NC port of the chip can be connected to GND externally.	

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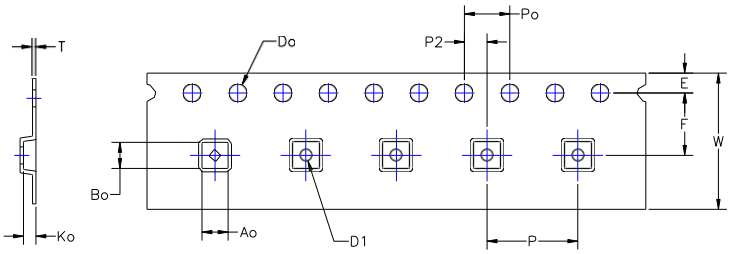
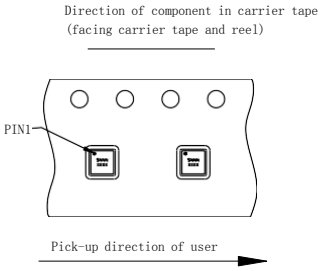
Packaging information



DIMENCWON	SPEC
W	12.00 +/-0.30
Do	ø 1.50 +0.10/-0.00
Po	4.00 +/-0.10
E	1.75 +/-0.10
D1	ø 1.00 MIN
Ao	2.30 +/-0.10
Bo	2.30 +/-0.10
P	8.00 +/-0.10
P2	2.00 +/-0.10
Ko	1.10 +/-0.10
T	0.30 +/-0.05
F	5.50 +/-0.05



Description:

1. Unit: mm
2. Material: Antistatic polyethylene
3. Color: Black
4. 10 Cumulative tolerance of center spacing (P0) of positioning holes ± 0.2

Matters needing attention

1. It is forbidden to try to clean the chip surface by wet chemical method.
2. This product is an electrostatic sensitive device, so pay attention to anti-static when storing and using.

1. Store in dry and nitrogen environment. If you have any questions, please contact the supplier