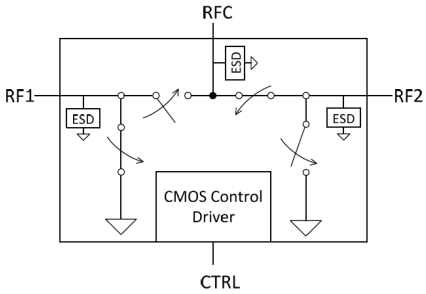
Performance Characteristics

- Operating frequency band: DC ~ 13GHz
- Low insertion loss: 0.8dB typical @ 10K to 6GHz
- High isolation: 50dB@10K~6GHz
  38dB@6GHz~8GHz
  30dB@8GHz~13GHz
- Package Size: 8-lead CFP

typical application

- base station communication
- wireless infrastructure
- automotive electronics
- Instrumentation

functional block diagram



summarize

The CWS9354S is a high isolation, low insertion loss, high linearity single-pole, double-throw switch.
The CWS9354S switches are available in a 8-lead CFP

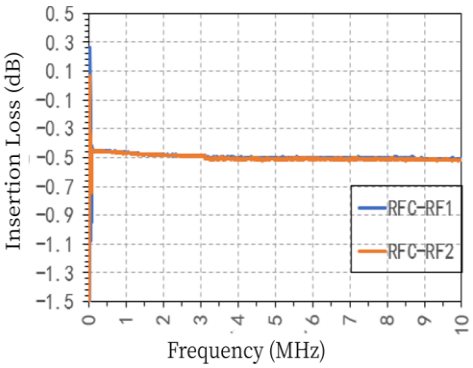
Electrical performance table (TA=+25°C, V_{CTRL}=0/3.3V, VSS=-2.4V, VDD-LS=3.3V)

Parameter name	test condition	minimum value	typical value	maximum values	unit (of measure)
RF Frequency Range		DC ~ 13			GHz
insertion loss	10K to 6GHz		0.8		dB
	6GHz to 8GHz		1.2		dB
	8GHz to 13GHz		1.8		dB
incommunicado	10K to 6GHz		50		dB
	6GHz to 8GHz		38		dB
	8GHz to 13GHz		30		dB
return loss	open state (math.)		-15		dB
	camouflage		-10		dB
phase coherence			0	1.5	
Amplitude consistency			0	0.1	dB
Bias Voltage (VDD)		3		5.3	V
Bias Current (IDD)				1	mA
Rise and fall time	10% to 90% RF output		30		ns
switching time	50% VCTRL to 10%/90% RF output		120		ns
Recommended Input Power	plug-in mode (math.)			31	dBm
	segregated state (physics)			26	dBm

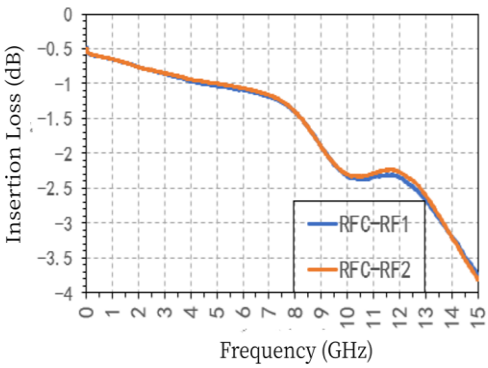
Note: 1. The lowest frequency of the test instrument to 10K, so only display 10K above the test data
2. The chip does not have an integrated DC/DC converter module, so the chip positive/negative power (VDD/VSS) must be added to the VSS range of -2.0 ~ -2.4 (V)

test curve

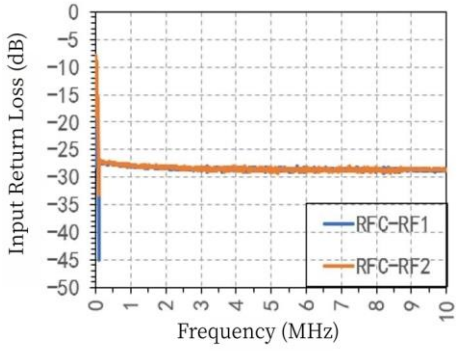
Insertion Loss vs. Frequency (@10K-10MHz)



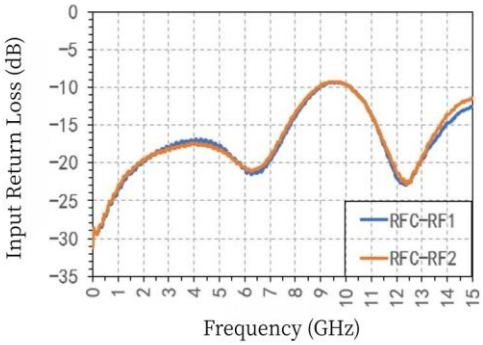
Insertion loss vs. frequency (@10M-15GHz)



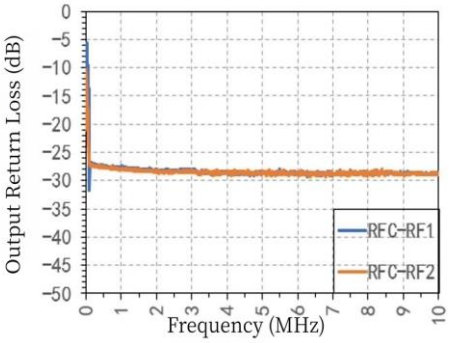
Input Return Loss VS Frequency (@10K-10MHz)



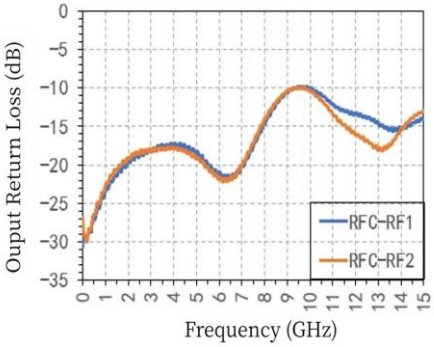
Input return loss vs. frequency (@10M-15GHz)



Output return loss vs. frequency (@10K-10MHz)



Output return loss vs. frequency (@10M-15GHz)



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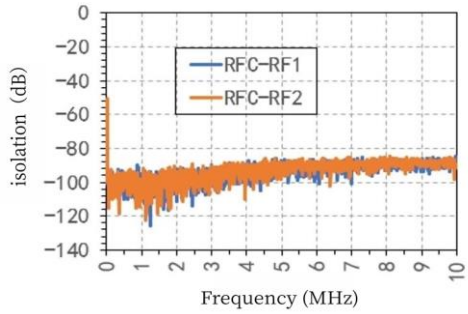
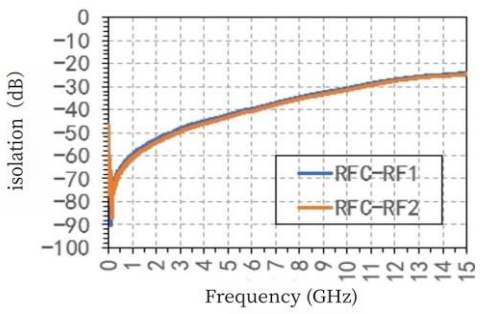
test curve

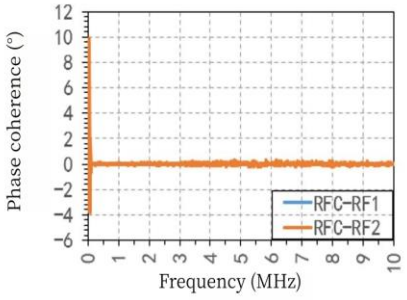
Isolation vs. Frequency (@10K-10MHz)



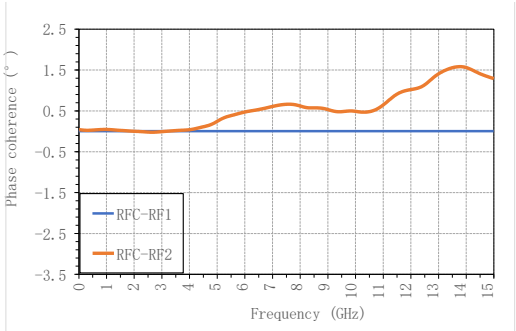
Isolation vs. Frequency (@10M-15GHz)



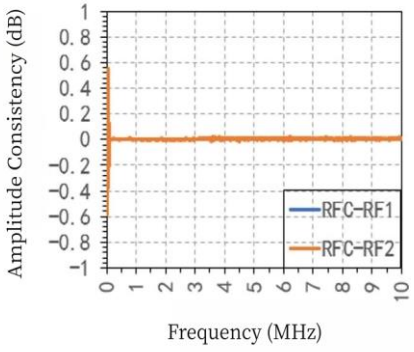
Phase coherence vs. frequency (@10K-10MHz)



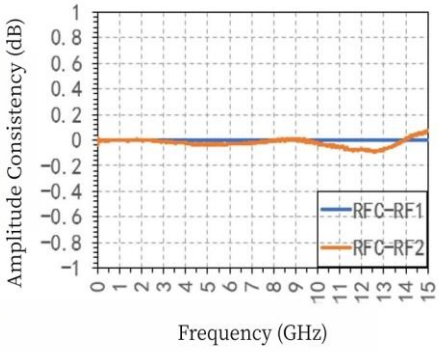
Phase coherence vs. frequency (@10M-15GHz)



Amplitude consistency vs. frequency (@10K-10MHz)



Amplitude consistency vs. frequency (@10M-15GHz)



Operating parameters

Negative power supply VSS	-2V to 2.4V
Bias voltage VDD	3V to 5.3V
Control voltage LS, VCTRL	0V to 0.3V (Low) 3V to 5.0V (High)
operating temperature	-45℃～+85℃

Absolute maximum rating

Bias Voltage VDD	-0.3V/5.6V
Control Voltage LS, VCTRL	-0.5 V/VDD+0.3V
Input power (insertion loss state)	33dBm
Input power (isolated state)	31dBm
Storage temperature	-65℃～+150℃

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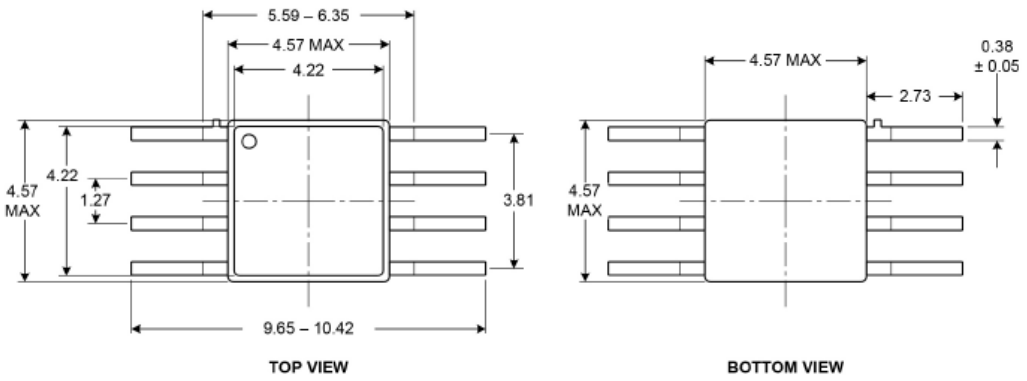
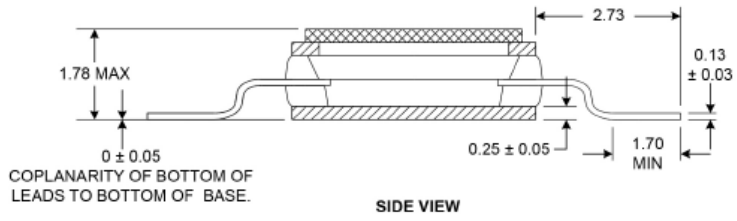
Package Drawing (dimensions are in millimeters)

8-lead CFP

Note: Bottom of the package is ground. Connecting the bottom of the package to ground is required.

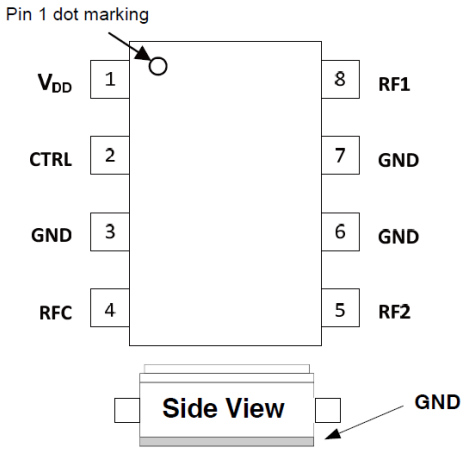




DIMS IN MM.
ALL TOLERANCES ARE +/- 0.127
UNLESS OTHERWISE STATED.
NOT TO SCALE

Rev. 97 170809
IIGNALB

Pin Configuration



Pin Description

Pin #	Pin Name	Description
1	V_{DD}	Nominal +3V supply connection.
2	CTRL	CMOS or TTL logic level: High = RFC to RF1 signal path. Low = RFC to RF2 signal path.
3	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
4	RFC	Common RF port for switch.*
5	RF2	RF2 port.*
6	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
7	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
8	RF1	RF1 port.*
GND	GND	Bottom of the package is ground. Connecting the bottom of the package to ground is required

Note: * All RF pins must be DC blocked with an external series capacitor or held at 0 VDC.

truth table

Control and bias inputs				signaling pathway state	
Negative Supply (VSS)	Bias Voltage (VDD)	Console (LS)	Console (VCTRL)	RFC to RF1	RFC to RF2
-2V	5V	High	Low	Off	on
-2V	5V	High	High	on	Off
-2V	5V	Low	Low	on	Off
-2V	5V	Low	High	Off	on

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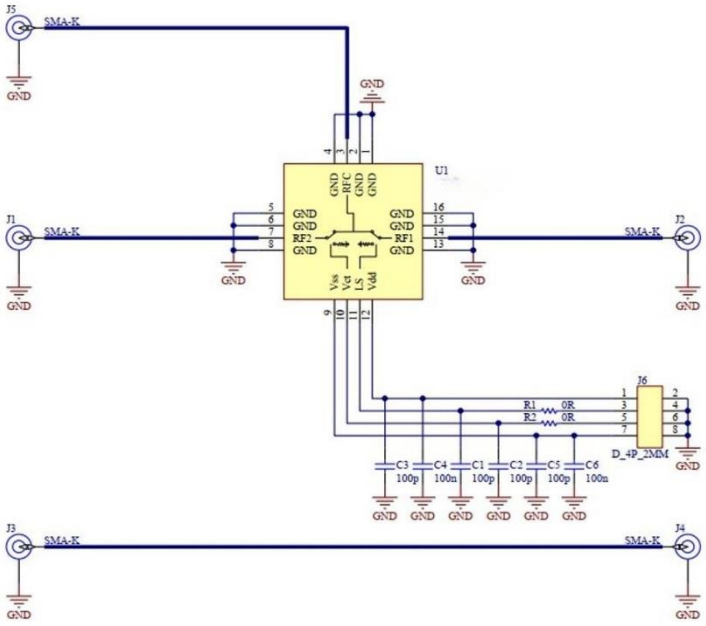
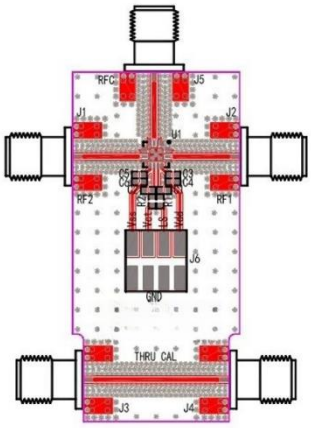
evaluation board





DeCWgnator	Description
C1, C2, C3, C5	100pF Ceramic Capacitor 0402
C4,C6	100nF Ceramic Capacitor 0402
J1, J2, J5	SMA-K PCB connectors
J6	4Pin 2mm DC Pin
R1, R2	0Ω Resistance 0402
U1	CWS9354S
J1,J2,J5 recommended SMA connector NJOYMAN D550B12E01-048	
NC indicates an unused port or the device is not soldered. The NC port on the chip is externally connected to GND.	

Circuit Board:Rogers4350B

The circuit board of the device application should be designed according to the design method of RF circuit, the signal line is designed according to 50Ω impedance, and the grounding pin of the package shell is close to the ground (similar to that in the figure), and there should be enough grounding holes to connect the top layer and the grounding ground of the bottom layer.