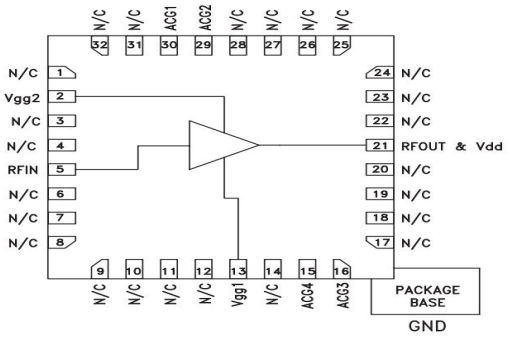
Performance characteristics:

- Frequency band:DC~20GHz
- Noise factor:1.5dB
- Gain：20dB
- Input and output return loss: >17dB/>10dB
- Output P1dB:19dBm
- Output IP3:33dBm
- Power supply:+8V@118mA
- 32 Lead 5x5 mm QFN Package: 25 mm^2

Functional Diagram



Product Description:

The CW-LN465SP5 is a GaAs MMIC ultra wideband low-noise amplifier chip with a frequency range covering DC~20GHz and a typical noise figure of 1.5dB throughout the band. the CW-LN465SP5 is powered by +8V.

Electrical parameters:(T_A=25℃，VD=+8V，VG=-0.25V)

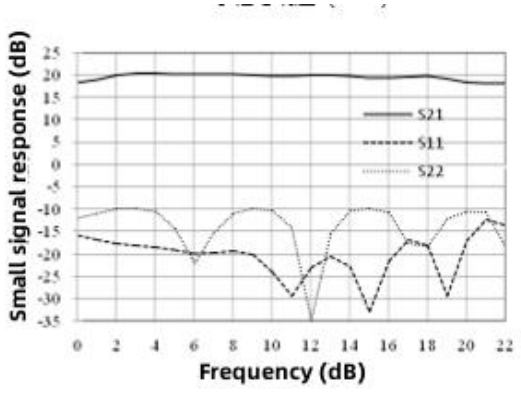
Indicators	Minimum value	Typical values	Maximum value	Unit
Frequency range	DC~20			GHz
Noise factor	1.2	1.5	3.2	dB
Gain	18.2	20	20.2	dB
Input Return Loss	17	-	-	dB
Output Return Loss	10	-	-	dB

Usage limitation parameters：(Exceeding any of the above maximum limits may result in permanent damage.)

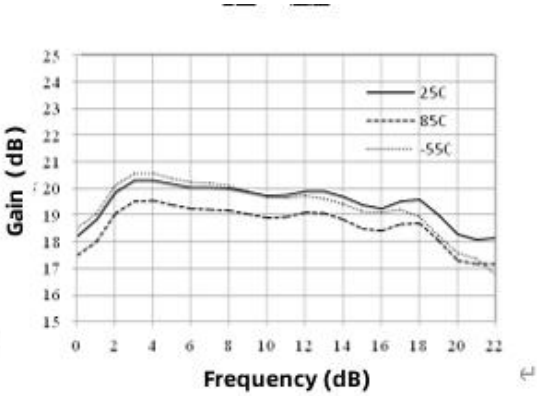
Input power	+23dBm
Control voltage	+9V
Storage temperature	-65℃~150℃
Operating temperature	-55℃~125℃

Typical curves:

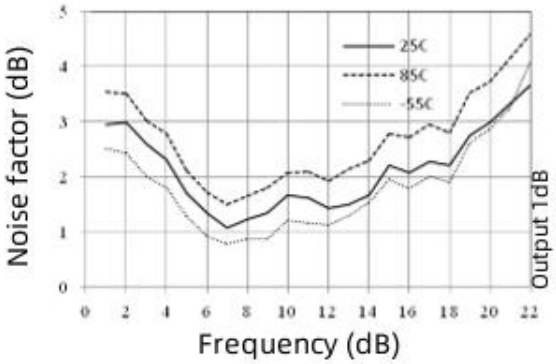
Small signal response (25°C)



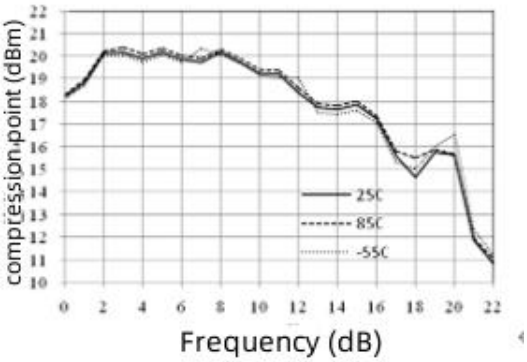
Gain Vs Temperature



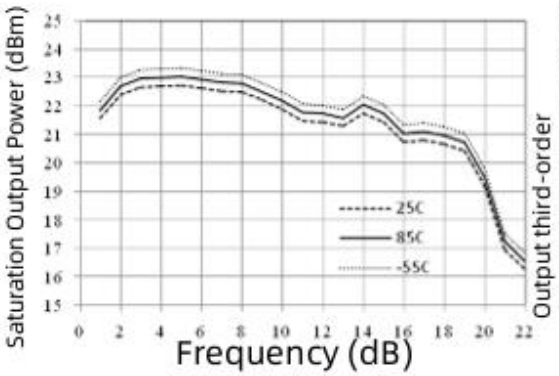
Noise factor Vs temperature



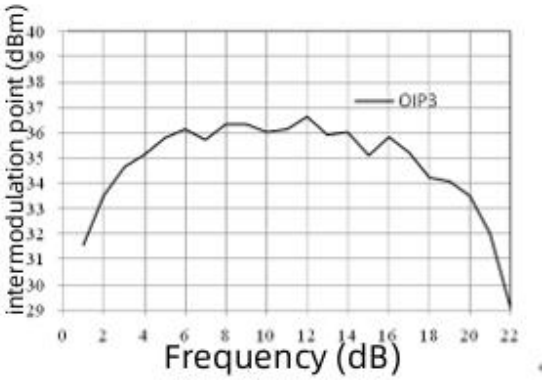
Output 1dB compression point Vs temperature



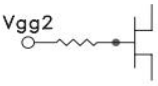
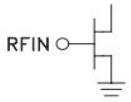
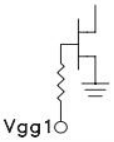
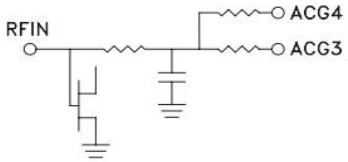
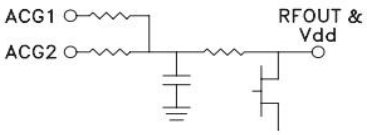
Output saturation power Vs Temperature



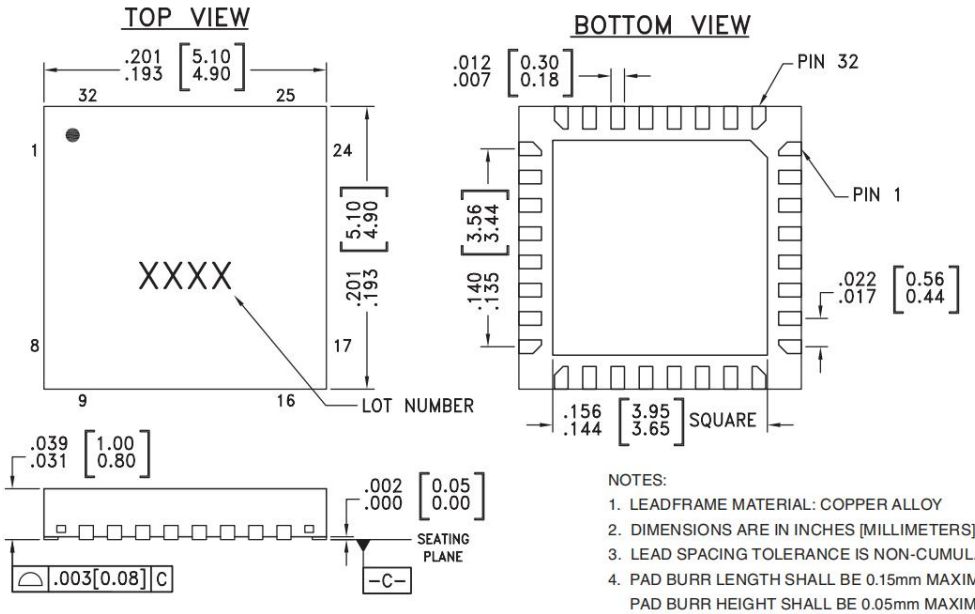
Output third-order intermodulation point (25°C)



PIN Description

Pin Number	Function	Description	Interface Schematic
1, 3, 4, 6 - 12, 14, 17, 18, 19, 20, 22 - 28, 31, 32	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
2	Vgg2	Gate Control 2 for amplifier. +1.5V should be applied to Vgg2 for nominal operation.	
5	RFIN	This pad is DC coupled and matched to 50 Ohms.	
13	Vgg1	Gate Control 1 for amplifier.	
15	ACG4	Low frequency termination. Attach bypass capacitor per application circuit herein.	
16	ACG3		
21	RFOUT & Vdd	RF output for amplifier. Connect the DC bias (Vdd) network to provide drain current (Idd). See application circuit herein.	
29	ACG2	Low frequency termination. Attach bypass capacitor per application circuit herein.	
30	ACG1		
Ground Paddle	GND	Ground paddle must be connected to RF/DC ground.	

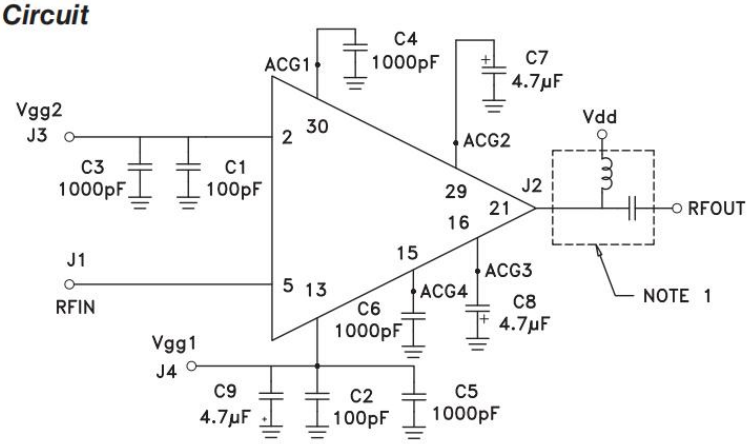
Outline drawing: (unit mm)



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Application Circuit



NOTE 1: Drain Bias (Vdd) must be applied through a broadband bias tee or external bias network.