### CW-PA0015005P

# GaAs MMIC Power Amplifier Chip, DC-15GHz

#### Performance characteristics:

Frequency range: DC-15GHz

Small signal gain: 18dB P-1dB: 25.5 dBm Psat: 26.5 dBm Power supply: + 8V @ 270mA 50Ohm input/output 100% on-chip test Chip size: 3.12 x 1.62 x 0.1 mm

#### Product Description:

CW-PA0015005P is a broadband amplifier chip based on GaAs technology. The frequency range covers DC-15GHz, the small signal gain is 18dB, and the Psat output power is 26.5 dBm. The chip via metallization process ensures good grounding, and the back side is metallized, which is suitable for eutectic sintering process.

Use the limit parameter 1		
Maximum leakage voltage	+ 14V	
Maximum input power	+ 20dBm	
Operating temperature	-55 ~ + 85 ° C	
Storage temperature	-65 ~ + 150 ° C	

"1" Exceeding any of the above maximum limits may cause permanent damage.

Electrical parameters (Ta=+25 ° C, Vd=+8V, Ids=270mA)				
Indicators	Minimum value	Typical value	Maximum value	Unit
Frequency range		DC-15		GHz
Small signal gain	-	18	-	dB
Gain flatness	± 1.6 dB		dB	
P-1dB	-	25.5	-	dBm
Psat	-	26.5	-	dBm
Input return loss	-	19	-	dB
Output return loss	-	22	-	dB
$*$ By tuning the Vg terminal voltage-2V $^{\sim}$ OV, the Vg terminal voltage is recommended to-0.65 V				

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Main index test curve

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#### GaAs MMIC Power Amplifier Chip, DC-



Reverse Isolation vs. Frequency



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#### **Exterior structure 2**



"2" The units in the drawing are all microns (tolerance for overall dimensions:  $\pm$  50um.)

Definition of bonding pressure point				
Bonding point serial number	Functional symbol	Functional description		
1	RF IN	The signal input terminal is externally connected with		
		a 50 ohm circuit, and a DC blocking capacitor needs to be added		
2	RF OUT, VD	The signal output end is externally connected with 50 ohm circuit, which needs to be added with DC blocking capacitor and externally connected with DC bias		
		Network to provide drain current. See the following application circuit or contact the manufacturer *		
3	VG1	The gate bias voltage of the amplifier needs to be externally connected with 100pF and 0.01 uF bypass capacitors		
4	VG2	The gate bias voltage of the amplifier needs to be externally connected with 100pF and 4.7 uF bypass capacitors		
5	VD2	External 100pF bypass capacitor is required and goes to ground		
6	VD1	External 4.7 uF bypass capacitor to ground		
Chip bottom	GND	The bottom of the chip should be in full and good contact with RF and DC ground		

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Suggested assembly drawing



#### Precautions for use

- The chip should be stored in a container with anti-static function and stored in nitrogen environment. And stored in an environment with a relative humidity of less than 30% at 10 °C ~ 30 °C.
- It is forbidden to try to clean the bare chip surface by wet chemical method.
- Please strictly comply with ESD protection requirements to avoid electrostatic damage of bare chips.
- Routine operation: Please use precision pointed tweezers to take bare chips. Avoid touching the chip surface with tools or fingers during operation.
- Suggestions for rack mounting operation: AuSn solder eutectic sintering process can be used for bare chip mounting. The mounting surface must be clean and flat.
- Sintering process: AuSn solder sheet with gold-tin ratio of 80/20 is recommended. The working face temperature reaches 255 °C, and the tool (vacuum chuck) temperature reaches 265 °C. When the high temperature mixture gas (nitrogen-hydrogen ratio is 90/10) is blown to the chip, the temperature at the top of the tool should be raised to 290 °C. Don't let the chip stay above 320 °C for more than 20 seconds. The rubbing time should not exceed 3 seconds.
- Suggestions for bonding operation: 0.025 mm (1mil) gold wire is used for spherical or wedge bonding. The thermo-ultrasonic bonding temperature was 150 °C. The pressure of spherical bonding cleaver is 40 ~ 50gf, and that of wedge bonding cleaver is 18 ~ 22gf. Use as little ultrasonic energy as possible. Bonding starts at the pad point on the chip and ends at the package (or substrate).