Performance characteristics

- Operating frequency range: 0.1 GHz ~ 6GHz
- Low insertion loss:

  0.45 dB @ 0.1 GHz ~ 2GHz (typ)

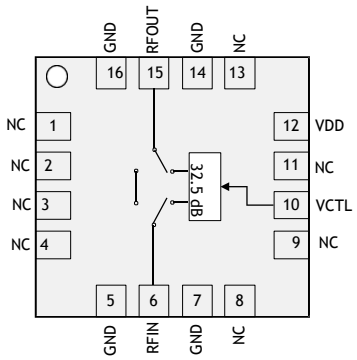
  0.5 dB @ 2GHz ~ 4GHz (typ)

  0.8 dB @ 4GHz ~ 6GHz (typ)
- Attenuation range: 32.5 dB
- Package size: 16-lead QFN, 3mmx3mm

Typical application

- Mobile infrastructure
- Satellite communication
- Microwave
- Instruments and meters

Functional block diagram



Overview

CWAT081SP3 is a one-bit numerically controlled attenuator chip with a frequency range of 0.1 GHz to 6GHz and an insertion loss of less than 0.8 dB typical. High attenuation accuracy. 3.3 V bias voltage.

The CWAT081SP3 attenuator is available in a 16-lead 3mmx3mm surface mount leadless plastic package. The pin pad is coated with Sn or NiPdAu.

Electrical performance table (TA=+25 ℃, VDD=3.3V)

Parameter name	Working conditions	Minimum value	Typical value	Maximum value	Unit
Frequency range		0.1		6	GHz
Insertion loss	0.1 GHz ~ 2GHz		0.45	0.6	dB
	2GHz ~ 4GHz		0.5	0.7	dB
	4GHz ~ 6GHz		0.8	1.2	dB
Attenuation range	0.2 GHz ~ 6GHz		32.5		dB
Attenuation accuracy	0.2 GHz ~ 1GHz	-0.5		1	dB
	1GHz ~ 5GHz	-1.5		0.5	dB
	5GHz ~ 6GHz	-0.5		2	dB
Input and output return loss			15		dB
Bias voltage (VDD)			3		V
Bias current (IDD)				1	mA
0.1 dB Compression Point Input Power (P0.1 dB)			25		dBm
Input third-order intercept point			TBD		dBm
Switching time (insertion loss state to attenuation state)	10% to 90% RF output		140		ns
Switching time (decay state to insertion loss state)	10% to 90% RF output		100		ns
Switching time	50% Vctl to 10%/90% RF output		200		ns
Recommended input power	Insertion loss state			30	dBm
	Attenuation state			24	dBm

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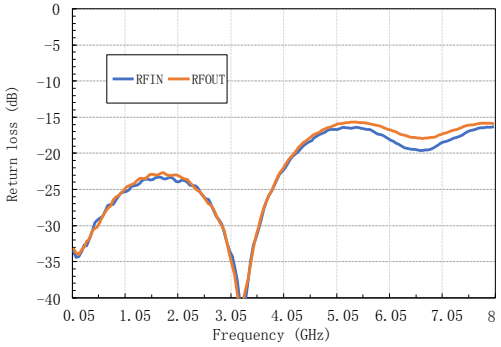
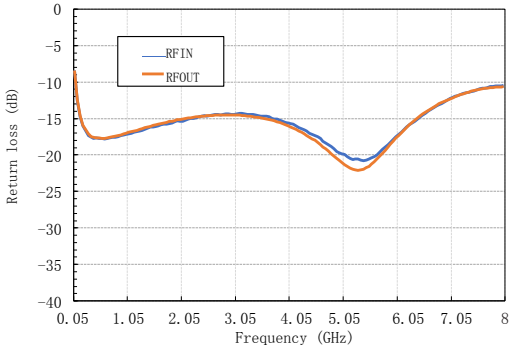
Test curve

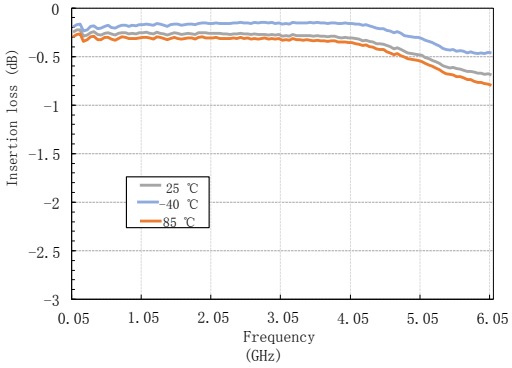
Attenuation error VS frequency



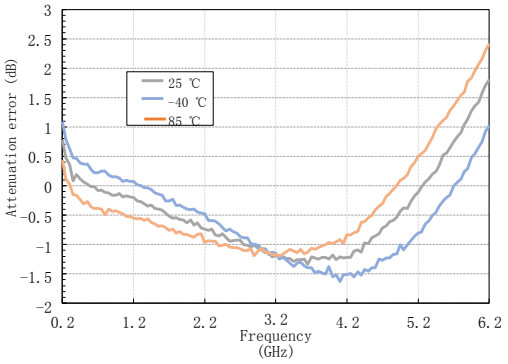
32.5 dB Return Loss VS Frequency



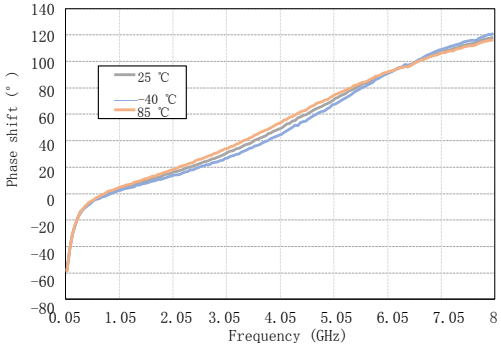
Insertion loss VS frequency



Attenuation error VS frequency



Phase shifted VS frequency



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Logic control truth table

Bias voltage VDD	Control input VCTL	Attenuator state
3.3 V	High	Insertion loss state
3.3 V	Low	Attenuation 32.5 dB

Operating parameters

Bias voltage VDD	3V ~ 3.3 V
Control voltage VCTL	0V ~ 0.3 V (Low) 3V ~ 3.3 V (High)
Operating temperature	-40 ℃ ~ + 85 ℃

Absolute maximum rating

Bias voltage VDD	-0.3 V ~ 3.6 V
Control voltage VCTL	-0.5 V ~ VDD+0. 3V
Input power	35dBm
Storage temperature	-65 ℃ ~ + 150 ℃

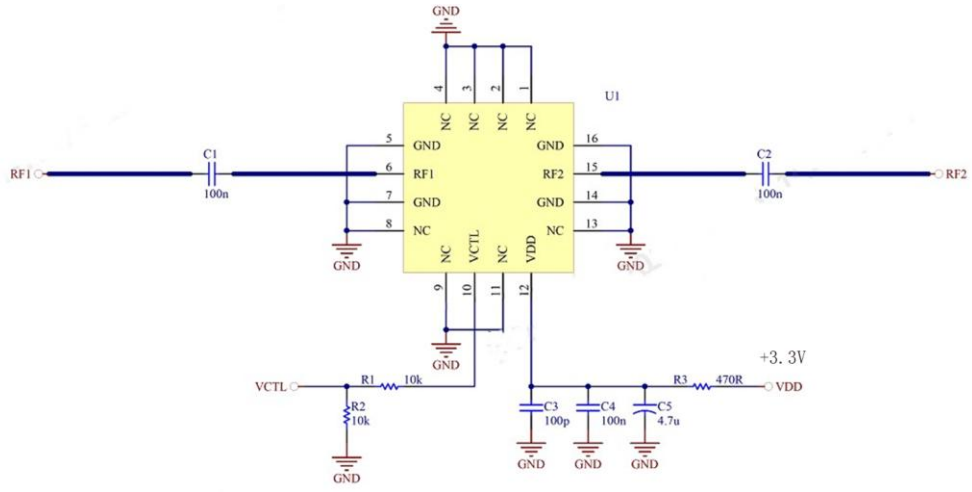
Encapsulation information

Model	Packaging material	Pad coating	MSL Rank [1]	Package ID [2]	Environmental protection requirements
CWAT081SP3	Green resin compound	Sn or NiPdAu	MSL 3	S081 XXXXX	RoHS compliant

[1] Maximum reflow soldering temperature 260 ℃

[2] XXXXX is the batch number

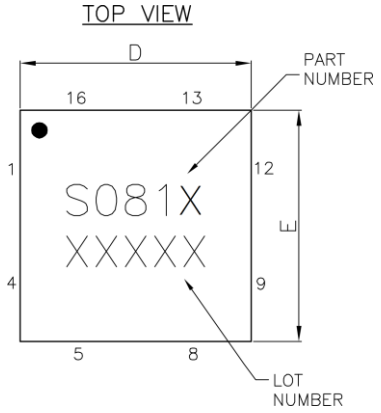
Typical application circuit

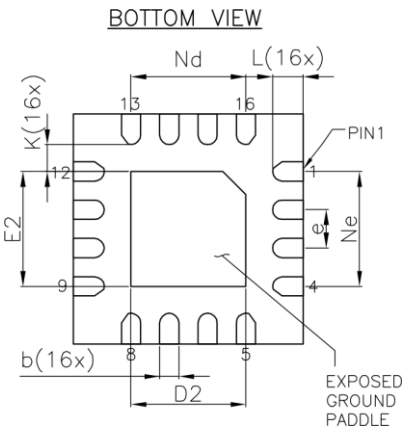


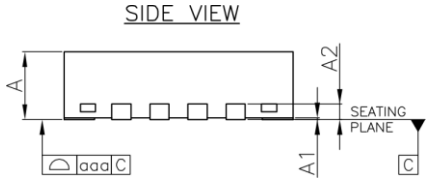
Note: The VDD port bias supply voltage is 3.3 V, and the resistance value of R3 resistor is not less than 470 Ω

Ensure that the voltage to the VDD port of the chip does not exceed 3.15 V

Overall dimensions







Description:

1. Unit: mm
2. Lead frame material: Copper alloy
3. Package surface warpage: no more than 0.05 mm
4. Connect all ground pins to PCB RF ground

Dimension Table (unit:mm)			
Symbol	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	---	0.05
A2		0.20Ref	
b	0.20	0.25	0.30
D	2.90	3.00	3.10
D2	1.40	1.50	1.60
e		0.50BSC	
Ne		1.50BSC	
Nd		1.50BSC	
E	2.90	3.00	3.10
E2	1.40	1.50	1.60
K	0.20	---	---
L	0.30	0.40	0.50
aaa		0.08	

Pin definition

Pin number	Functional symbol	Functional description	Pin number	Functional symbol	Functional description
1	NC	Vacancy	9	NC	Vacancy
2	NC	Vacancy	10	VCTL	Control port
3	NC	Vacancy	11	NC	Vacancy
4	NC	Vacancy	12	VDD	Bias voltage
5	GND	Radio frequency ground	13	NC	Vacancy
6	RFIN	Radio frequency port	14	GND	Radio frequency ground
7	GND	Radio frequency ground	15	RFOUT	Radio frequency port
8	NC	Vacancy	16	GND	Radio frequency ground

It is recommended that all NC pins be connected to RF ground when in use

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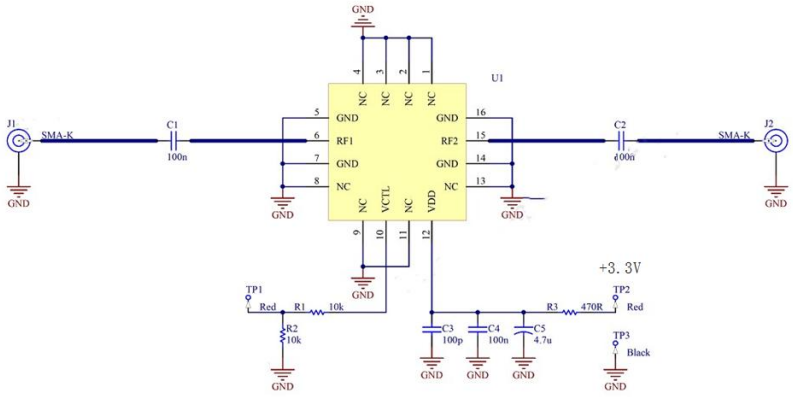
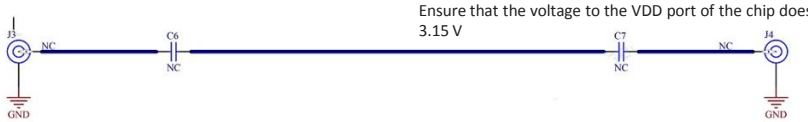
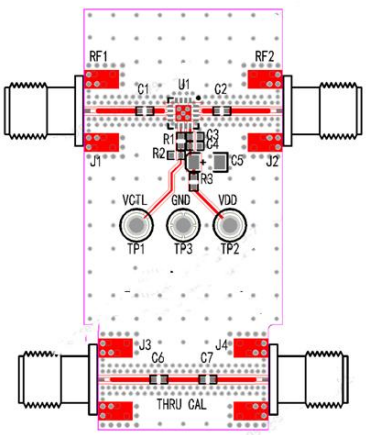
Evaluation board



Note: TP2 port bias supply voltage is 3.3 V, and R3 resistor resistance value is not less than 470 Ω

Ensure that the voltage to the VDD port of the chip does not exceed 3.15 V



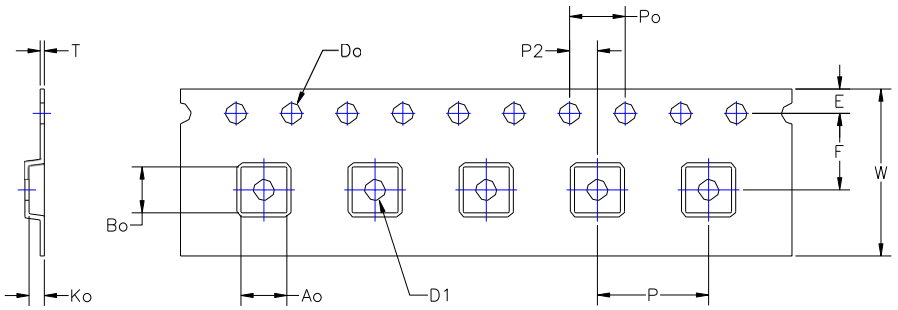


Circuit board material: Rogers 4350B

The circuit board used in the device shall be designed according to the design method of RF circuit, the signal line shall be designed according to the impedance of 50 ohm, and the grounding pin of the package housing shall be grounded nearby (similar to the figure), and there shall be enough grounding holes connecting the top layer and the bottom layer.

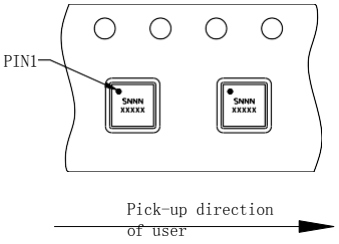
Designator	Description
C1, C2, C4	Multilayer Ceramic Capacitor 0402 100nF
C3	Multilayer Ceramic Capacitor 0402 100pF
C5	Tantalum capacitor 1206 4.7 uF
J1, J2	SMA-K PCB Connector
R1, R2	Resistance 0402 10k Ω
R3	Resistance 0402 470 Ω
TP1, TP2, TP3	DC Test Terminal
U1	CWAT081SP3
SMA-K connector of Nanjing Aowen D550B12E01-023 is recommended for J1 and J2	
NC means that ports are not used or the device is not soldered. The NC port of the chip can be connected to GND externally.	

Packaging information



DIMENSION	SPEC
W	12.00 +/-0.30
Do	Ø 1.50 +0.10/-0.00
Po	4.00 +/-0.10
E	1.75 +/-0.10
D1	Ø 1.50 MIN
Ao	3.30 +/-0.10
Bo	3.30 +/-0.10
P	8.00 +/-0.10
P2	2.00 +/-0.10
Ko	1.10 +/-0.10
T	0.30 +/-0.05
F	5.50 +/-0.05

Direction of component in carrier tape
(facing carrier tape and reel)



Description:
1. Unit: mm
2. Material: Antistatic polyethylene
3. Color: Black
4. 10 Cumulative tolerance of center spacing (P0) of positioning holes ± 0.2

Matters needing attention

1. It is forbidden to try to clean the chip surface by wet chemical method.
2. This product is an electrostatic sensitive device, so pay attention to anti-static when storing and using.
3. Storage in dry environment.

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