Performance Characteristics:

- Operating frequency: DC~20GHz
- Insertion loss: 5.5dB
- Attenuation range: 0.5~31.5dB
- Attenuation Additional Phase Shift: -6°~+4°
- RMS: 0.4dB
- RF1/RF2 standing wave: 1.8/1.8
- Input and output impedance: 50Ω
- Package size: 3mmx3mm

FUNCTIONAL BLOCK DIAGRAM

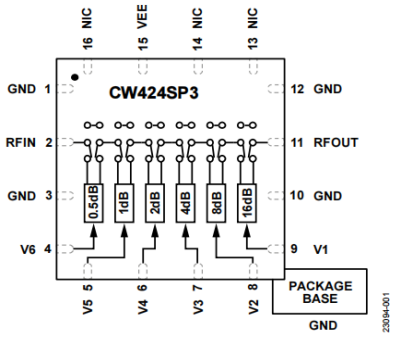


Figure 1.

Product Description:

CW424SP3is a 6-bit numerical control attenuator chip operating at DC~20GHz with typical insertion loss of 5.5dB. It adopts 0V/+5V logic control and requires external -5V power supply bias, which is characterized by small insertion loss, high attenuation accuracy, small size and easy integration.

Electrical parameters: (T_A = 25°C, 0V/+5V control)

norm		minimum value	typical value	maximum values	unit (of measure)
frequency range			DC~20		GHz
Attenuation range			0.5~31.5		dB
insertion loss		-	5.5	-	dB
Attenuate Additional Phase Shift		-6	-	+4	°
attenuation	0.5 dB bit	-	0.5	-	dB
	1 dB bit	-	1.0	-	dB
	2dB bit	-	2.0	-	dB
	4dB bit	-	4.1	-	dB
	8dB bit	-	8.1	-	dB
	16dB bit	-	16.2	-	dB
RMS		-	0.4	-	dB
RF1/RF2 standing wave		-	1.8/1.8	-	-

Control truth table: (VEE=-5V, control bit voltage 0/+5V)

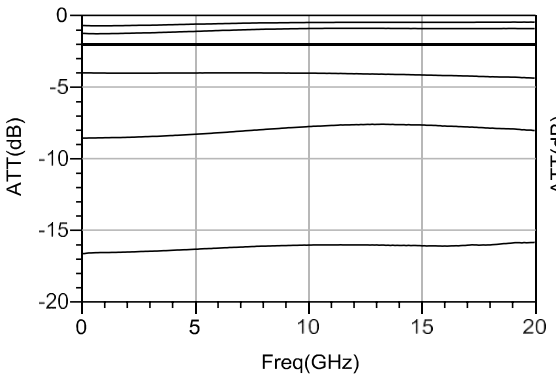
control input						state of affairs
IN1	IN2	IN3	IN4	IN5	IN6	
0V	0V	0V	0V	0V	0V	consultation
0V	0V	0V	0V	0V	5V	0.5dB
0V	0V	0V	0V	5V	0V	1dB
0V	0V	0V	5V	0V	0V	2dB
0V	0V	5V	0V	0V	0V	4dB
0V	5V	0V	0V	0V	0V	8dB
5V	0V	0V	0V	0V	0V	16dB
5V	5V	5V	5V	5V	5V	31.5dB

Use the restriction parameter:

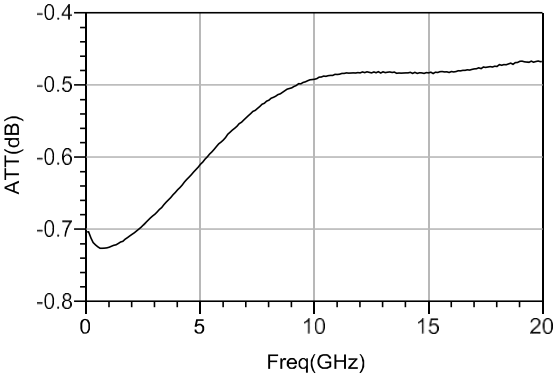
Input power Pin	23dBm
Control voltage range	0V~+5V
Storage temperature	-65℃~+150℃
operating temperature	-55℃~+85℃

Typical curve: (TA=+25°C)

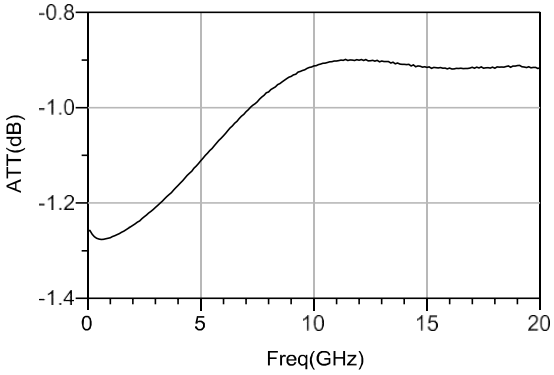
Basic attenuation state



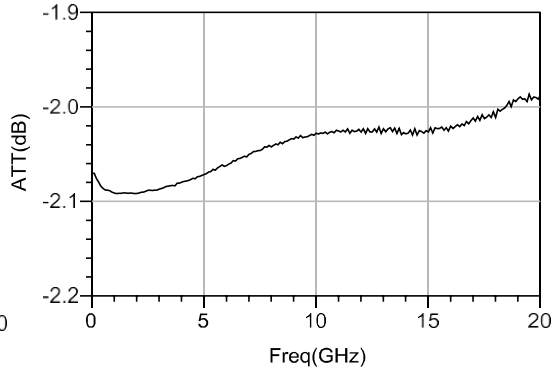
0.5dB attenuation state



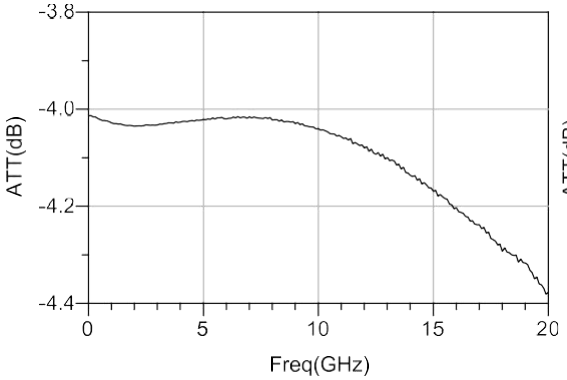
1dB attenuation state



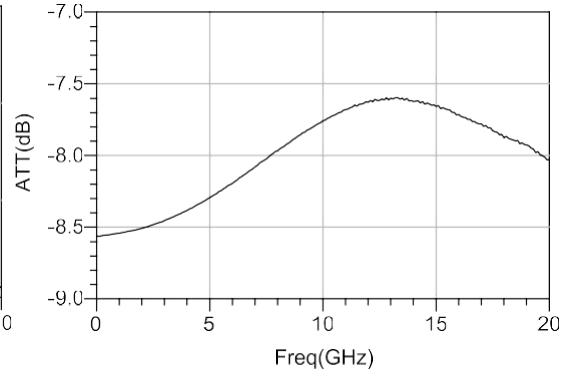
2dB attenuation state



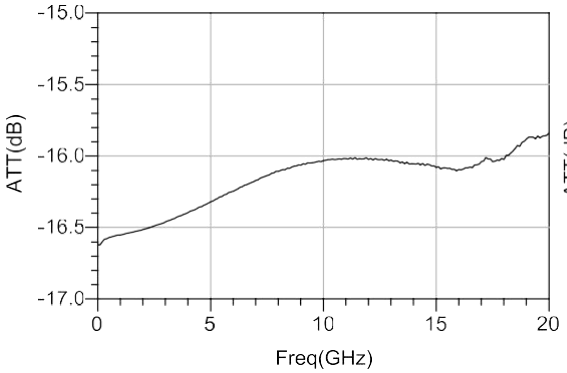
4dB attenuation state



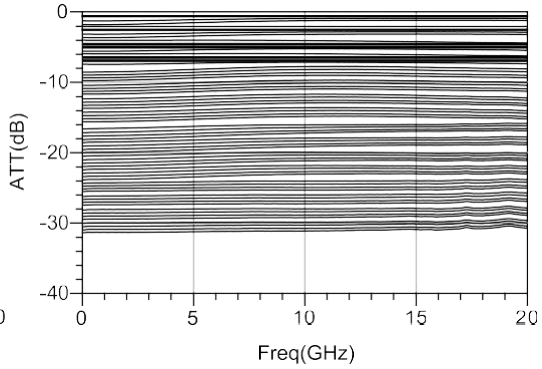
8dB attenuation state



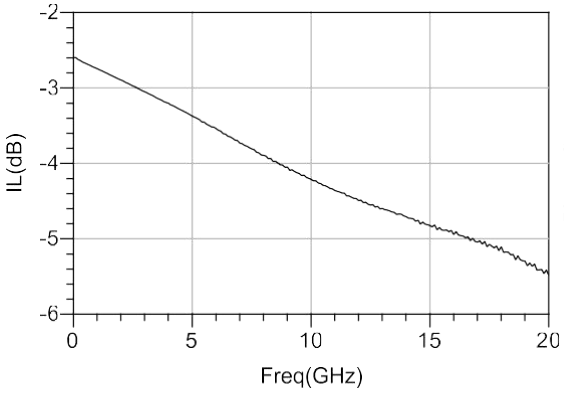
16dB attenuation state



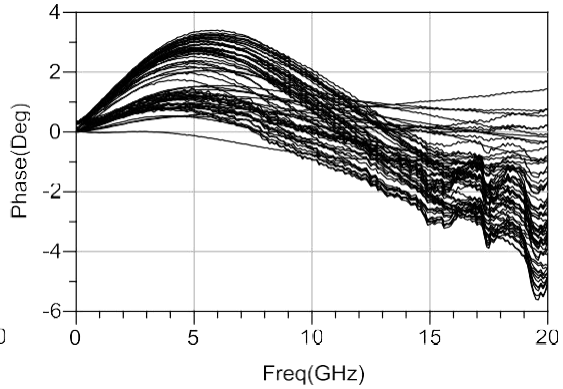
All attenuation state



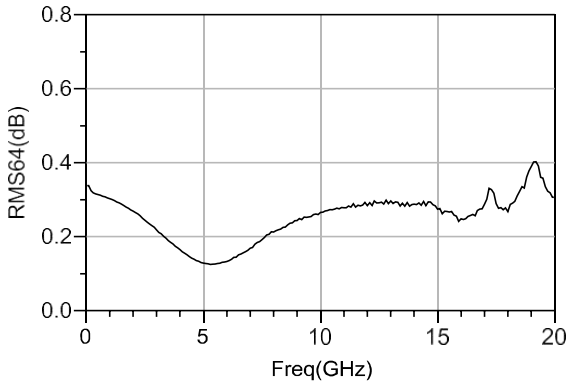
Insertion Loss



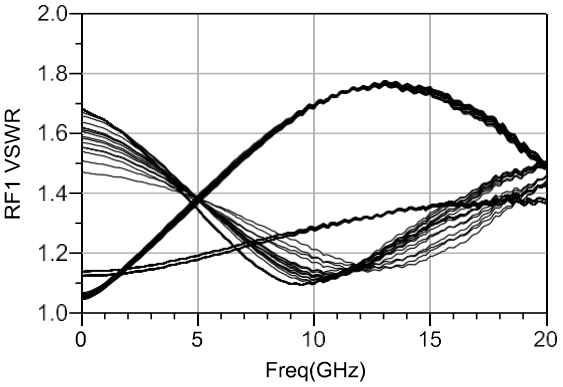
Attenuation Additional Phase Shift



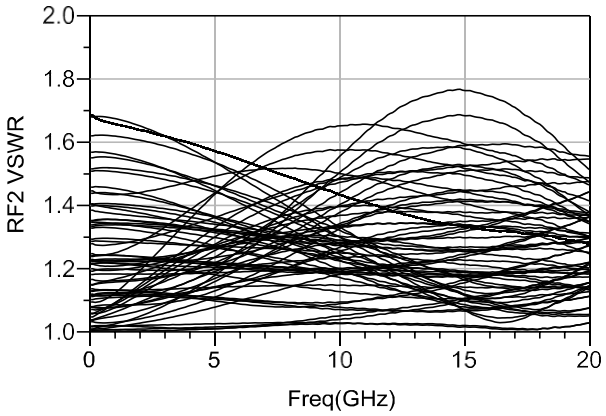
64-state attenuation accuracy



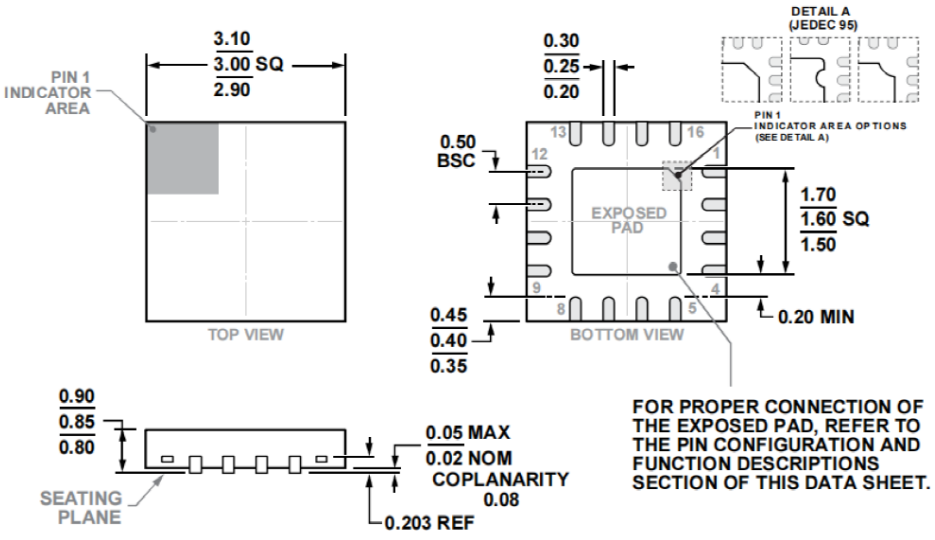
RF1 standing wave



RF2 standing wave



OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VEED-4

Bonding pressure point definition:

Pressure point number	functional symbol	Functional Description
2	RF1	RF signal input/output terminals, external 50Ω system, no isolation capacitors inside the chip
5	RF2	RF signal input/output terminals, external 50Ω system, no isolation capacitors inside the chip
8, 15	VEE	Bias voltage terminal, external -5V, two VEE internal connectivity, use only need to connect either end of the external.
9~14	IN	DC control signal, external 0V/+5V voltage
1, 3, 4, 6, 7, 16	GND	Ground pressure point for probe testing
Backside of the chip	GND	The bottom of the chip needs to be in good contact with RF and DC ground.

Instructions for use:

Storage: The chip must be placed in a container with static protection and stored under a nitrogen atmosphere.

Cleaning treatment: Bare chips must be operated and used in a purified environment, and it is prohibited to use liquid cleaners to clean the chips.

Electrostatic protection: Please strictly comply with the ESD protection requirements to avoid electrostatic damage to the device.

Routine operation: Use a vacuum chuck or precision pointed tweezers to pick up the chip. Avoid touching the chip surface with tools or fingers during operation.

Mounting operation: Chip mounting can use AuSn solder eutectic welding or conductive adhesive bonding process. The mounting surface must be clean and flat.

Bonding operation: 2 bonding wires (25um diameter gold wire recommended) are used for each input and output, and a bonding wire length of less than 250um is optimal. It is recommended to use as little ultrasonic energy as possible. Bonding starts at the pressure point on the chip and ends at the package (or substrate).