CWS4306sp4

DC-4GHz RF Digital Step Attenuator

Product Description

The CWS4306sp4 is a 50Ω,5-bit RF Digtial Step Attenuator designed for use in 2G/3G/4G/5G wireless infrastructure and other performance RF applications.The CWS4306sp4 covers a 31dB attenuation range in 1dB steps.The CWS4306sp4 maintains high linearity and low power consumption from DC through 4 GHz.An integrated digital control interface supports serial programming of the attenuation.

The CWS4306sp4 is housed in a miniature 20-pin, 4mmx4mm QFN package. A functional block diagram is shown in Figure1.A package and pin-out view of CWS4306sp4 is shown in Figure 2.

Applications

- Cellular,2G/3G/4G/5G
- Repeaters
- Microwave Radio & Test Equipment
- General Purpose Wireless

Features

- 50Ω impedance
- Attenuation:1dB steps to 31dB
- Monotonicity:1dB up to 4 GHz
- High attenuation accuracy: <1.5dB@ any Bit
- High linearity: +52 dBm IIP3
- Single-supply operation
- Small QFN(20-pin,4mm x4mm) package

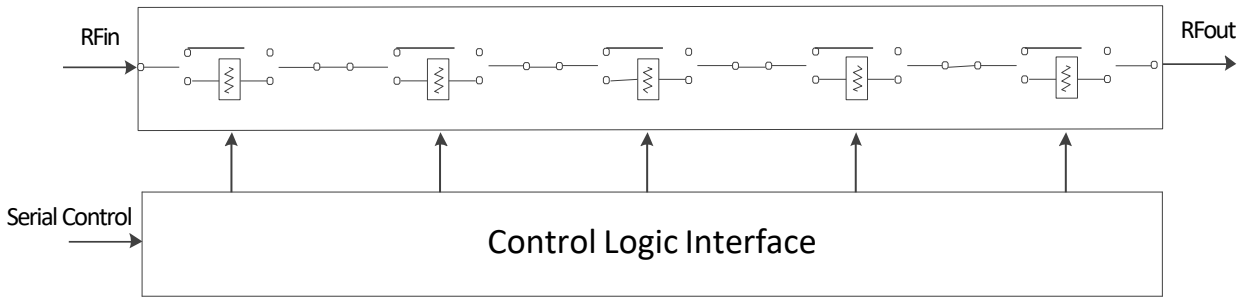


Figure 1. Functional Block Diagram

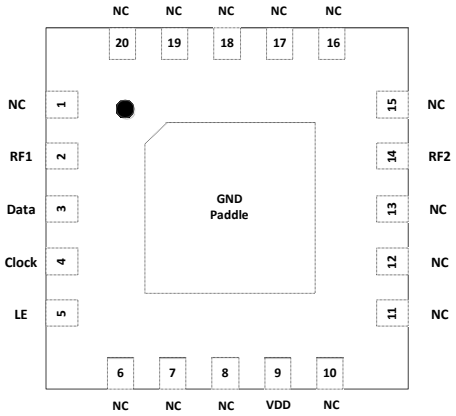


Figure 2. Pin-out – 20-Pin QFN

Table 1. Pin Description

Pin#	Name	Description	Pin	Name	Description
1	NC	No connection	11	NC	No connection
2	RF1	RF port 1	12	NC	No connection
3	Data	Serial interface data inpu	13	NC	No connection
4	Clock	Serial interface clock	14	RF2	RF port 2
5	LE	Latch Enable input	15	NC	No connection
6	NC	No connection	16	NC	No connection
7	NC	No connection	17	NC	No connection
8	NC	No connection	18	NC	No connection
9	VDD	Power supply	19	NC	No connection
10	NC	No connection	20	NC	No connection

Table 2. Absolute Maximum Rating

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage	VDD		+4.0	V
Voltage on any input	V_I		VDD+0.3	V
Input power (50 Ω load)	P_{IN}		+24	dBm
Storage temperature	T_{STG}	-40	+150	℃
Operating ambient temperature	T_{op}	-40	+85	℃
Junction temperature	T_J		150	℃
ESD Rating – Human Body Model	ESD		5000	V

Table 3. Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
supply voltage	VDD	2.7	3.0	3.3	V
supply current	I_{DD}		200		uA
Control logic:					
High	V_{HI}	0.7xVDD			V
Low	V_{LO}			0.3xVDD	V
Digital Input Leakage	I			1	uA

Table 4. Electrical Specifications (TA=+25℃,VDD=3.0V)

Parameters	Test Conditions	Frequency	Minimu	Typical	Maxim	Units
Operation Frequency			DC		4000	MHz
Insertion Loss				1.5	2.5	dB
Attenuation Accuracy	Any Bit or Bit Combination	DC-4GHz			1.5	dB
P1dB[1]			30	34		dBm
Input IP3	Two-tone inputs +18dBm			52		dBm
Return Loss				14	20	dB
Switching Speed	50% control to 1.0dB of final value				1	us

Note1: Note Absolute Maximum in Table 2.

Typical Performance Data（25℃，VDD=3.0V）

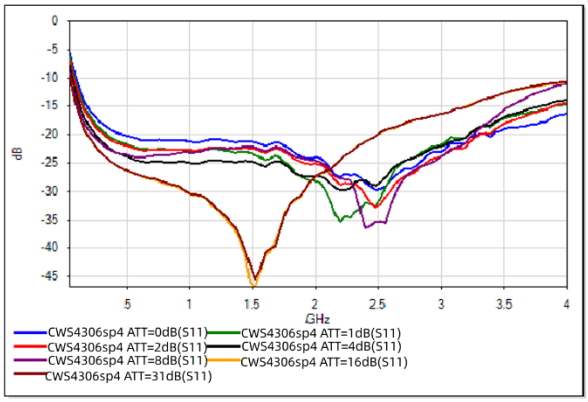


Figure 3. Input Return Loss at Major Attenuation Steps

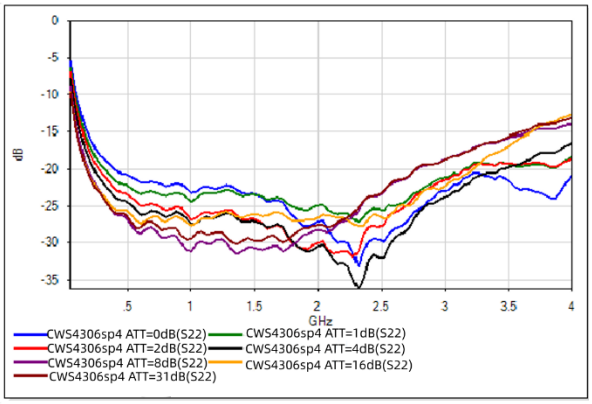


Figure 4. Output Return Loss at Major Attenuation Steps

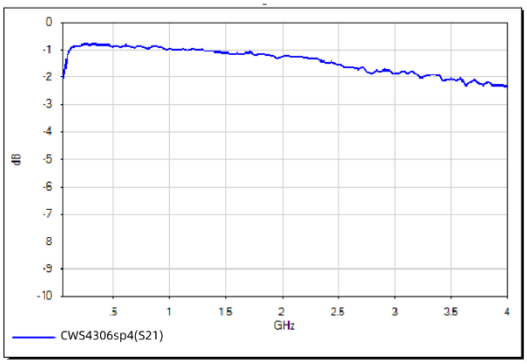


Figure 5. Insertion Loss

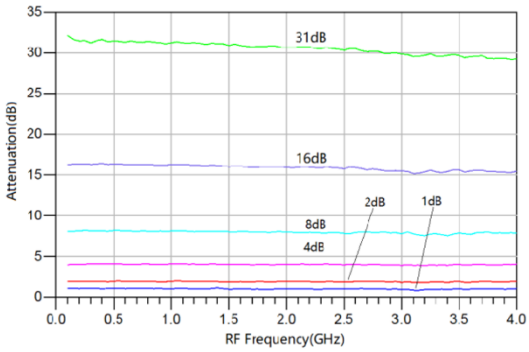


Figure 6. Attenuation at Major steps

Programming Options

Serial Interface

The serial interface is a 5-bit serial-in, parallel-out shift register buffered by a transparent latch. It is controlled by three CMOS-compatible signals: Data, Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH,the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by Figure 3 (Serial Interface Timing Diagram) and Table 6 (Serial Interface AC Characteristics).

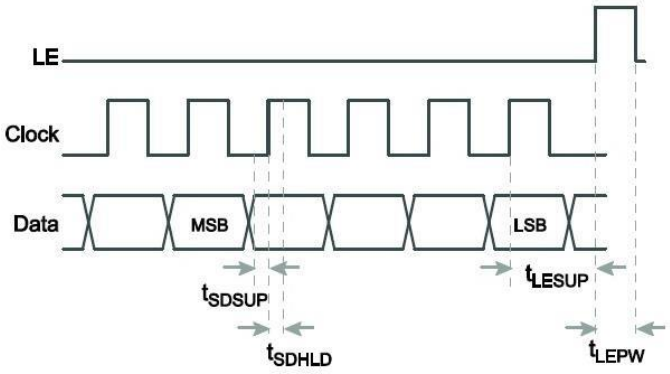


Figure 7. Serial Interface Timing Diagram

Table 5. 5-Bit Attenuator Serial Programming

B5	B4	B3	B2	B1
C16	C8	C4	C2	C1

MSB(first in) LSB(last in)

Table 6. Serial Interface AC Characteristics

Symbol	Parameter	Minimu	Maxim	Units
fClk	Serial data clock frequency		10	MHz
tClkH	Serial clock HIGH time	30		ns
tClkL	Serial clock LOW time	30		ns
tLESUP	LE set-up time after last clock falling edge	10		ns
tLEPW	LE minimum pulse width	30		ns
tSDSUP	Serial data set-up time before clock rising edge	10		ns
tSDHLD	Serial data hold time after clock falling edge	10		ns

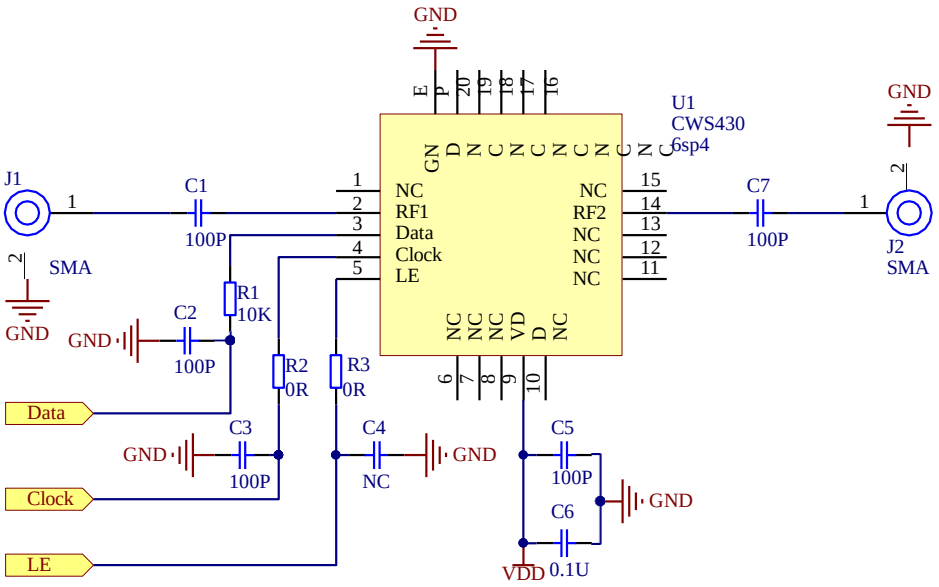


Figure 8. Application Schematic

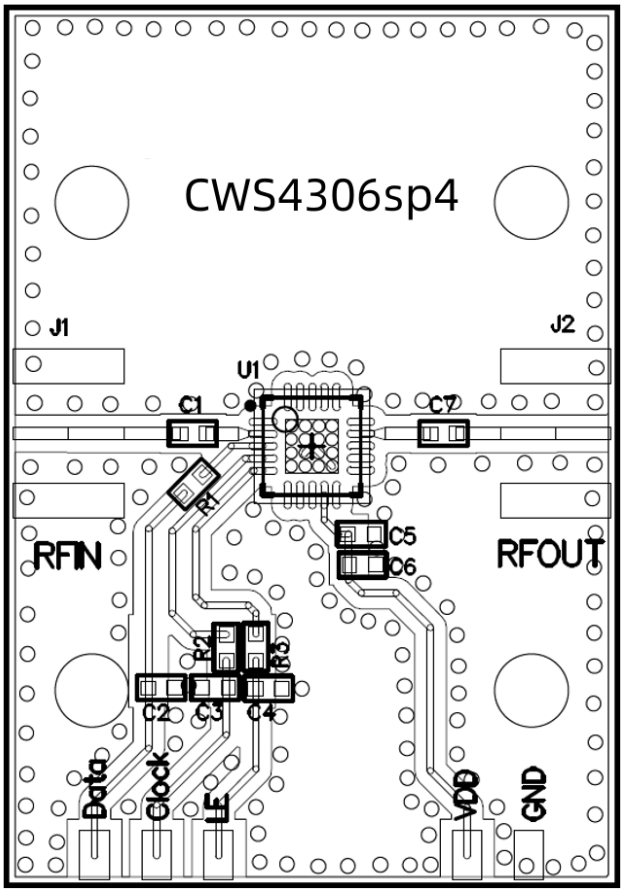
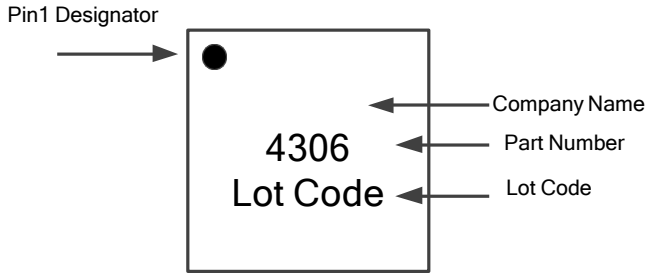
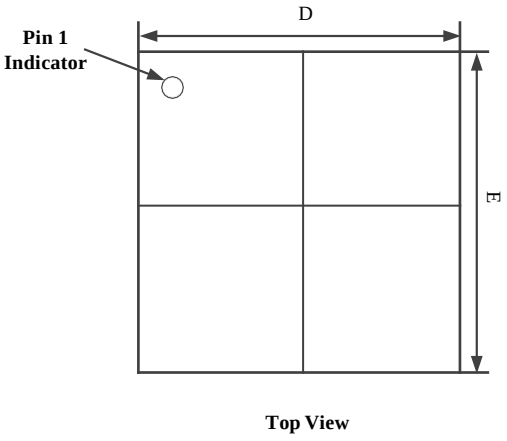


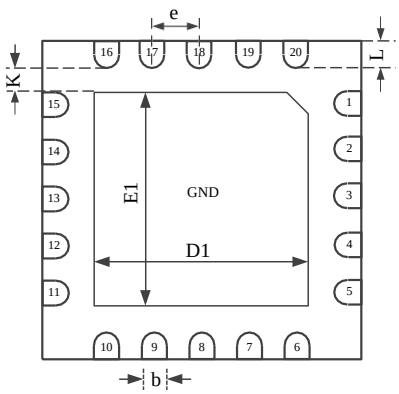
Figure 9. Evaluation Board Assembly Drawing

Package diagram:

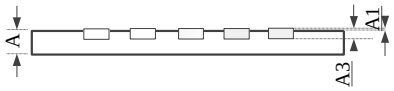




Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		
	Min.	Nom	Max.
A	0.8	0.9	1.0
A1	0	0.02	0.05
A3		0.08	
D		4.00BSC	
E		4.00BSC	
D1	2.3	2.45	2.55
E1	2.3	2.45	2.55
K	0.2	---	---
b	0.18	0.25	0.30
e		0.50BSC	
L	0.30	0.40	0.50

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
CWS4306sp4 DSA	CWS4306sp4	EVB-CWS4306sp4-01

Document Change History

Revision	Date	Notes
1.0	Apr. 28, 2022	Created.