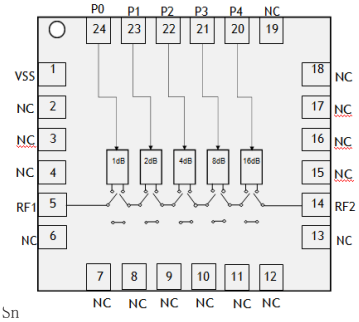
Performance Features

- Operating frequency range: DC ~ 35GHZ
- Low insertion loss: 3.5dB@DC~20GHz(typ)
  5.0dB@20GHz～32GHz(typ)
  7.0dB@32GHz～35GHz(typ)
- Attenuation range: 1dB～31dB
- Package size: 24-pin QFN, 4mm*4mm

Typical Applications

- Mobile Infrastructure
- Satellite Communications
- Microwave
- Instrumentation

Functional Block Diagram



Overview

CWAT044SP4 is a five-bit CNC attenuator chip with frequency range covering DC to 35GHz and insertion loss below 7.0dB typical. High attenuation accuracy, 1dB attenuation step, -5V bias voltage.

The CWAT044SP4 type attenuator is a QFN-24L, 4mm*4mm size package with Sn plated pads.

Electrical performance table (TA=+25℃,VSS=-5V)

Parameter Name	Working conditions	Minimum value	Typical values	Maximum value	Unit
Frequency range			DC ~ 35		GHz
insert loss	DC～20GHz		3.5		dB
	20GHz～32GHz		5.0		dB
	32GHz～35GHz		7.0		dB
Attenuation range		1		31	dB
Attenuation accuracy	DC～35GHz			2.3	dB
Input and output return loss			12		dB
Bias Voltage (VSS)		-5.2		-4.8	V
Bias current (Iss)	DC～35GHz		5		mA
Control current			5		mA
Input 0.1dB compression point power (P0.1dB)	DC～35GHz		TBD		dBm
1dB compression point input power (P1dB)			5		mA
1dB compression point input power (P1dB)	DC～35GHz		TBD		dBm
Input third-order intercept points	full decay state		23.5		dBm
Switching time (insertion loss state to maximum decay state)	straightforward state		26		dBm
Switching time (maximum decay state to insertion loss state)			TBD		dBm
Switching time	50% Vctl to 10%/90% RF output		80		ns
Recommended input power			20		dBm

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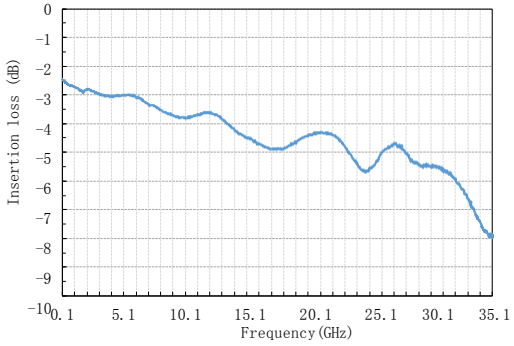
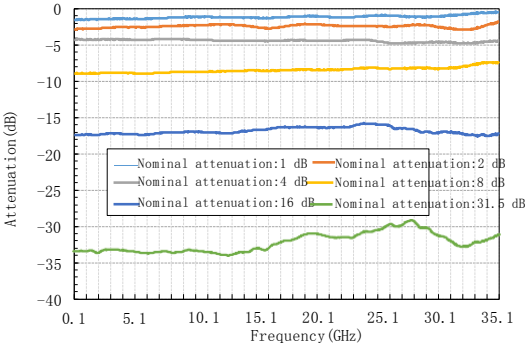
Test Curve

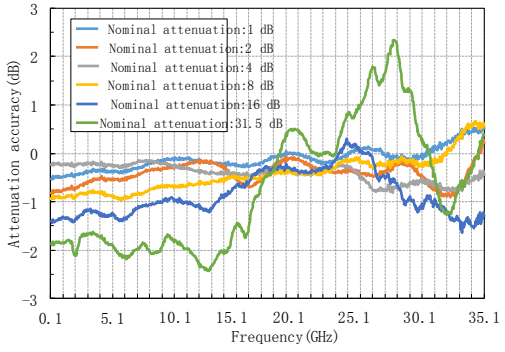
Insertion loss vs. frequency



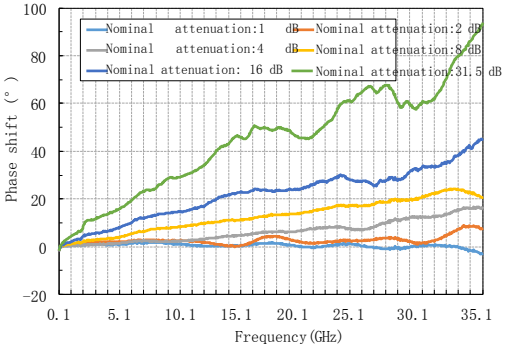
Attenuation amount vs. frequency



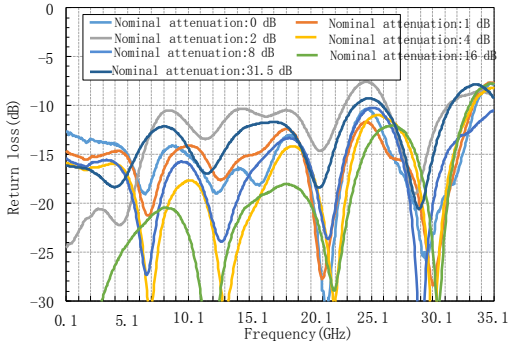
Attenuation accuracy vs. frequency



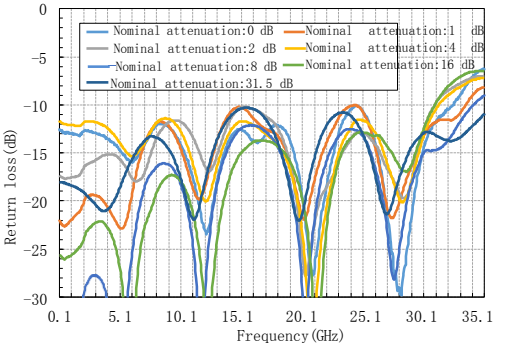
Phase shift vs. frequency



Input return loss vs. frequency



Output return loss vs. frequency



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Working parameters

Bias voltage VSS	-4.8V to -5.2V
Control voltage	0V～0.8V (Low) 3V to 5V (High)
Operating temperature	-40℃～+85℃

Control ports: P4, P3, P2, P1, P0

Absolute maximum rating

RF input power	+25dBm
Bias voltage VSS	-6.5V
Control voltage	-VSS-0.5V
Storage temperature	-65℃～+150℃
ESD (HBM)	TBD

Package Information

Model	Packaging Materials	Solder plate plating	MSL level [1]	Package identification [2]	Environmental requirements
CWAT044SP4	Green resin compounds	Sn	MSL 3	SO44 XXXXX	RoHS compliant

[1] Maximum reflow temperature 260° C
[2] XXXXX is the lot number

Truth Table

VSS	Control Port					Decay state
	1dB P0	2dB P1	4dB P2	8dB P3	16dB P4	RF1 to RF2
-5V	+5V	+5V	+5V	+5V	+5V	straightforward state
	0	+5V	+5V	+5V	+5V	1dB
	+5V	0	+5V	+5V	+5V	2dB
	+5V	+5V	0	+5V	+5V	4dB
	+5V	+5V	+5V	0	+5V	8dB
	+5V	+5V	+5V	+5V	0	16dB
	0	0	0	0	0	31dB

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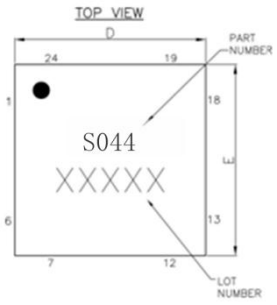
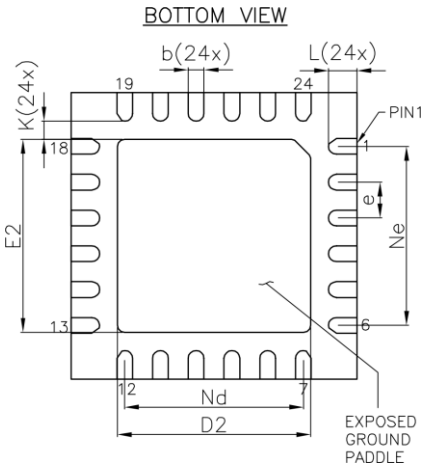
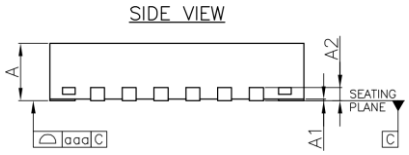
Dimension







Description:

1. Unit: mm
2. Lead frame material: copper alloy
3. Package surface warpage: not more than 0.05mm
4. All ground pins please connect PCB RF ground

Dimension Table (unit:mm)			
Symbol	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	---	0.05
A2		0.20Ref	
b	0.20	0.25	0.30
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
e		0.50BSC	
Ne		2.50BSC	
Nd		2.50BSC	
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
K	0.20	---	---
L	0.30	0.40	0.50
aaa		0.08	

Pin Definition

Pin Number	Function Symbols	Function Description	Pin Number	Function Symbols	Function Description
1	VSS	Negative Power	13	NC	Vacant
2	NC	Vacant	14	RF2	RF 2 ports
3	NC	Vacant	15	NC	Vacant
4	NC	Vacant	16	NC	Vacant
5	RF1	RF 1 port	17	NC	Vacant
6	NC	Vacant	18	NC	Vacant
7	NC	Vacant	19	NC	Vacant
8	NC	Vacant	20	P4	Control port 4
9	NC	Vacant	21	P3	Control port 3
10	NC	Vacant	22	P2	Control port 2
11	NC	Vacant	23	P1	Control port 1
12	NC	Vacant	24	P0	Control Port 0

All NC pins are recommended to be connected to RF ground when in use

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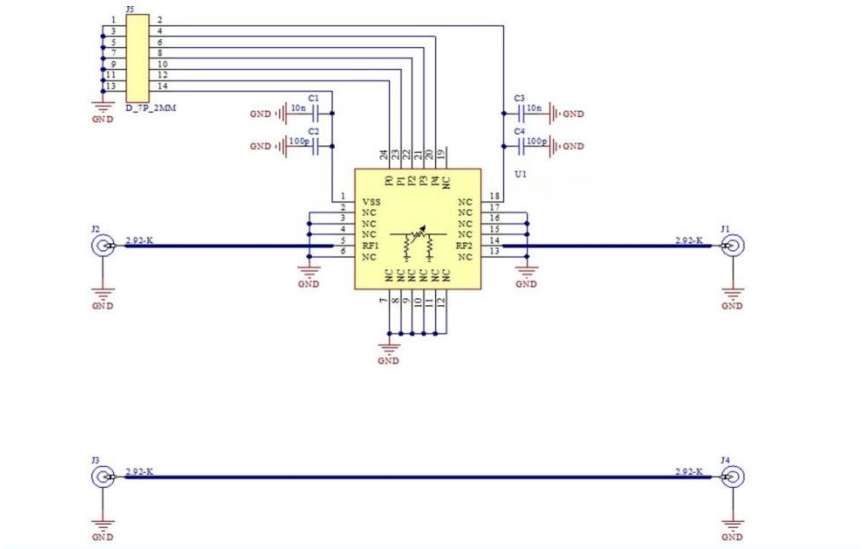
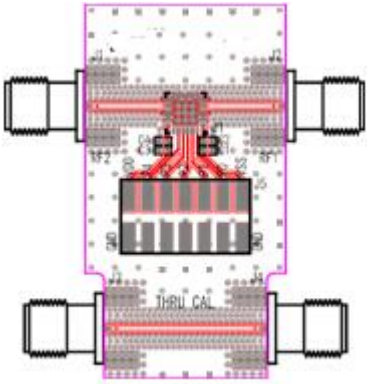
Evaluation Boards





Designator	Description
C1, C3	Multilayer Ceramic Capacitor 10nF 0402
C2, C4	Multilayer ceramic capacitor 100pF 0402
J1, J2, J3, J4	2.92-K connector Nanjing Aowen D360B12E01-023
J5	D_7P_2MM DC pin
U1	CWAT044SP4

Circuit board material: Rogers 4350B

The circuit board of the device application should be designed according to the RF circuit design method, the signal line should be designed according to the 50 ohm impedance, and the ground pin of the package shell should be grounded nearby (similar to the figure), and there should be enough grounding holes to connect the top and bottom ground layers.