phase-locked ring

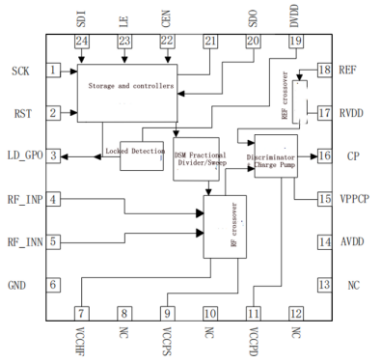
Performance Characteristics

- frequency range
  Integer mode: 0.1~26GHz
  Fractional mode: 0.2~18GHz
- Normalized bottom noise:
  Integer mode: -235dBc/Hz Fractional mode: -227dBc/Hz
- Maximum phase identification frequency:
  Integer mode: 300MHz Fractional mode: 150MHz
- 3.3V power supply
- QFN24 4*4 Package Format

Typical Application

- wireless infrastructure
- point-to-point radio
- point-to-multipoint radio
- Test equipment and instruments

Functional Block Diagram



Summary

The CWPL219SP4 is an integrated integer N-division and fractional N-division phase-locked loop that supports 0.1~26GHz RF bandwidth inputs, with a maximum discriminate frequency of 300MHz (integer mode)/150MHz (fractional mode).

The internal reference divider, phase discriminator, charge pump, feedback divider, and delta-sigma fractional frequency divider modulator modules are integrated.

Electrical performance table （TA=+25℃, VCCHF=VCCPS=VCCPD=AVDD=VPPCP=RVDD=DVDD=VccDIG=3.3V）

test parameter	descriptive	unit (of measure)	Indicator parameters		
			minimum value	typical value	maximum values
REF parameters					
REF Frequency Range	Input Sine Wave	MHz	10		500
Input power range		dBm	0		11
R crossover ratio			1		16383
Frequency range of phase detection	integer mode	MHz	1		300
	fractional part of a number mode	MHz	5		150
RF parameters					
RF Frequency Range	integer mode	GHz	0.1		26①
	fractional part of a number mode	GHz	0.2		18
RF Feedback Power	integer mode	dBm	-15		10
	fractional part of a number mode	dBm	-15		10
N Crossover Ratio	integer mode		20		32767
	fractional part of a number mode		23		32767
Charge Pump Parameters					
Minimum CP Current		mA		0.03	
Maximum CP Current		mA		7.6	
CP leakage current		mA		TBD	
Basic Functional Parameters					
Supply Current	3.3V	mA		130	
Shutdown current		mA		11	

Note: Integer mode 25GHz and above is recommended at TA=70° C and below.

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Electrical Performance Table

test parameter		descriptive	unit (of measure)	Indicator parameters		
				minimum value	typical value	maximum values
PLL Closed Loop Parameters						
normalized background noise①		integer mode. PD=100MHz, VCO=10GHz	dBc/Hz		-235	
		Fractional mode. PD=100MHz, VCO=10.001GHz	dBc/Hz		-227	
flicker noise②		Integer mode @ 10 kHz offset	dBc/Hz		-127	
Phase noise	Phase noise @ 1kHz	PD = 100 MHz Pin=10dBm, Fout=10GHz Integer mode VCO Model: CWV100SP4	dBc/Hz		-96	
	Phase noise @ 10kHz		dBc/Hz		-106	
	Phase noise @ 100kHz		dBc/Hz		-110	
	Phase noise @ 1MHz		dBc/Hz		-118	
	Phase noise @ 10MHz		dBc/Hz		-142	
Phase noise	Phase noise @ 1kHz	PD = 100 MHzPin=10dBm, Fout=10. 001 GHz Decimal pattern VCO Model: CWV100SP4	dBc/Hz		-95	
	Phase noise @ 10kHz		dBc/Hz		-103	
	Phase noise @ 100kHz		dBc/Hz		-106	
	Phase noise @ 1MHz		dBc/Hz		-119	
	Phase noise @ 10MHz		dBc/Hz		-140	
stray	integer-boundary spuriousness	REF=100MHz, RF=10.00001GHz	dBc/Hz		-45	
	forensic hybridization	REF=100MHz, RF=10GHz	dBc/Hz		-95	
Lock detection function		Pull high after locking (Locked output voltage: 2.8V~VDD, Unlocked output voltage: GND~0.4V)				

Note① : Normalized low noise refers to the bottom noise of the PLL itself, which is calculated by the formula:

$$PN_{floor} = Floor\ FOM + 10\log(f_{pd}) + 20\log(f_{vco}/f_{pd})$$

Note② : Flicker noise calculation formula:

$$PN_{flick} = Flicker\ FOM + 20\log(f_{vco}) - 10\log(f_{offset})$$

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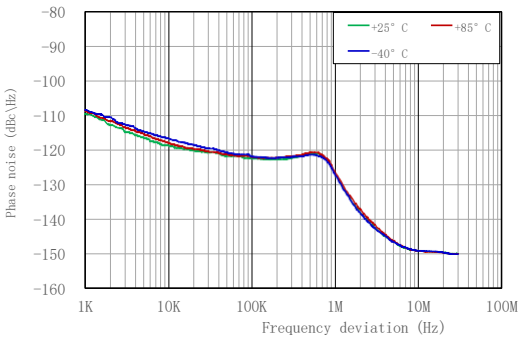
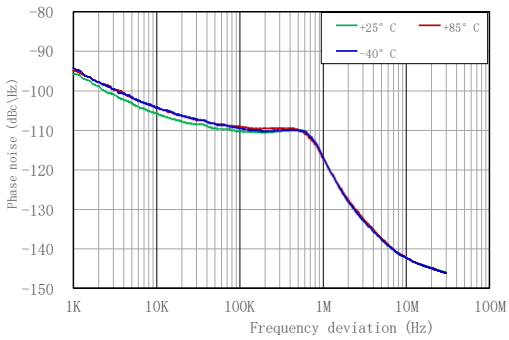
Test curve (Integer mode PRF=0dBmPREF=10dBmPD=100MHzLoop bandwidth=600KHz)

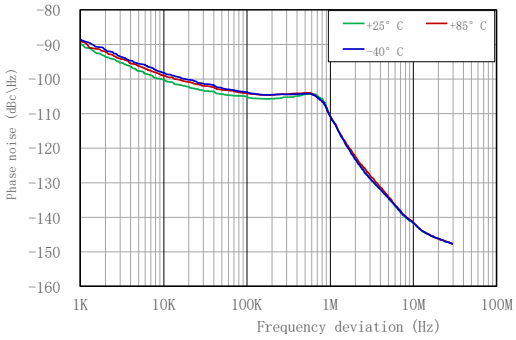
Phase Noise vs. Frequency Bias (Fout=2GHz)



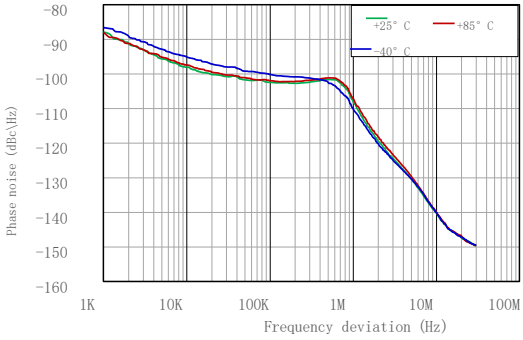
Phase Noise vs. Frequency Bias (Fout=10GHz)



Phase Noise vs. Frequency Bias (Fout=20GHz)

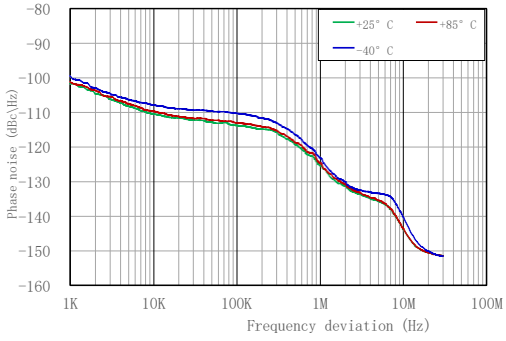


Phase Noise vs. Frequency Bias (Fout=26GHz)

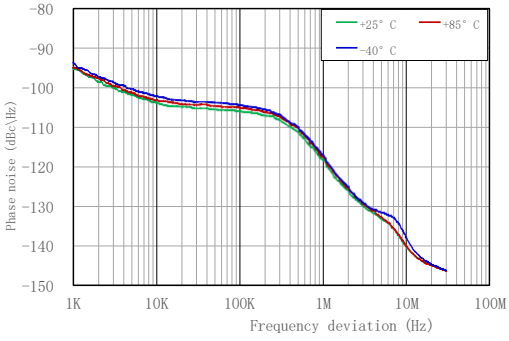


Test curve (Fractional mode PRF=0dBmPREF=10dBmPD=100MHz Loop bandwidth = 300KHz)

Phase Noise VS Frequency Bias
(Fout=5.001GHz)

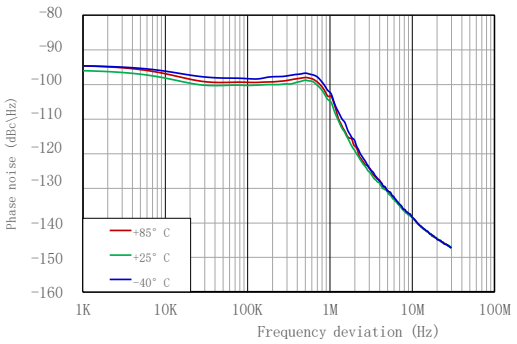


Phase noise vs. frequency
deviation (Fout = 10.001 GHz)



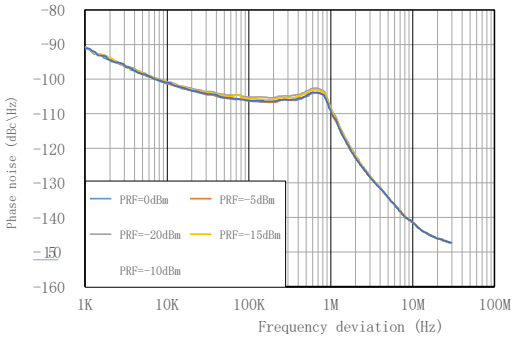
Test curve (Fractional mode PRF=0dBmPREF=10dBmPD=100MHz)

Phase Noise VS Frequency Bias (Fout=18.001GHz)



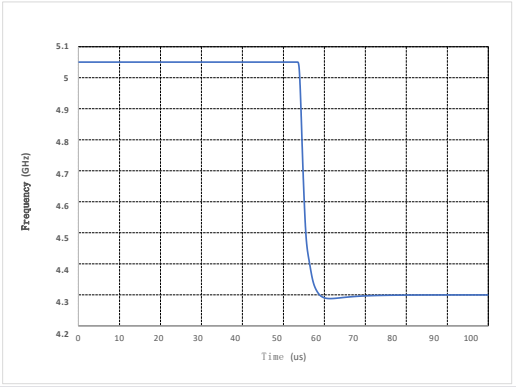
Test curve (Integer mode PREF=10dBmPD=100MHzLoop bandwidth=900KHz)

Phase Noise vs. Frequency Bias (Fout=20GHz)

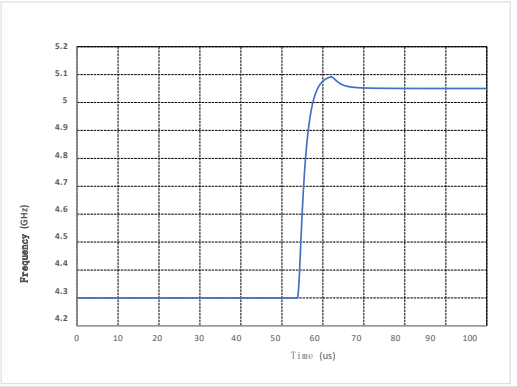


Frequency switching time

Frequency switching VS time (PD=10MHz)



Frequency switching VS time (PD=10MHz)



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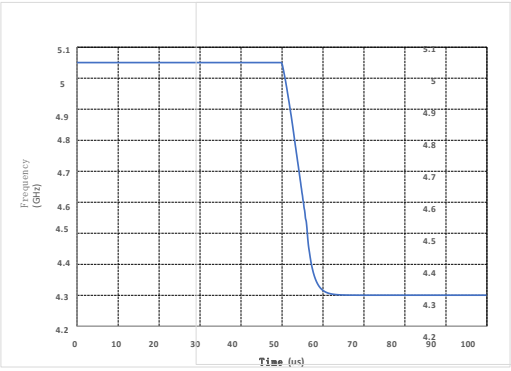
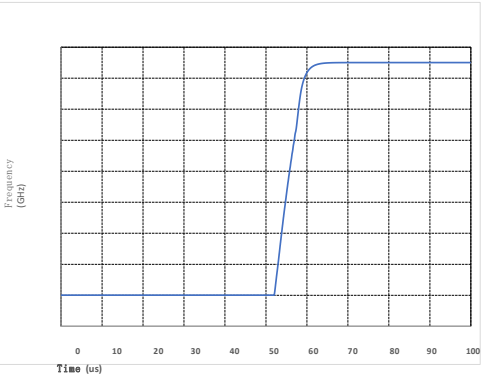
Frequency switching time

Frequency switching VS time (PD=100MHz)



Frequency switching VS time (PD=100MHz)



Absolute maximum rating

RF Input Power	+13dBm
VCCHF, VCCPS, VCCPD, AVDD, VPPCP, RVDD, DVDD, VccDIG	3.6V
Storage temperature	-65℃~+150℃
operating temperature	-40℃~+85℃
ESD (HBM)	TBD

Package Information

model number	package material	Pad plating	MSL rating [1]	Package identification [2]	environmental requirement
CWPL219SP4	Green resin compounds	NiPdAuAg	MSL 3	S219 XXXXX	RoHS compliant

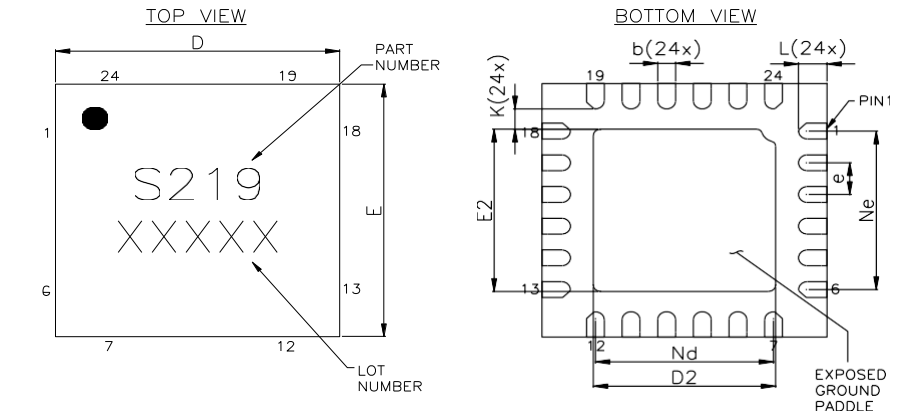
[1] Maximum reflow temperature 260° C

[2] XXXXX is the lot number

Pin Definitions

PIN number	name (of a thing)	descriptive
1	SCK	SPI serial clock input, 3.3/1.8V TTL level.
2	RST	Register reset port, internal integrated 80kΩ pull-down, 3.3/1.8V TTL level
3	LD_GPO	LD output port, can also be used as a selective output port for some internal signals
4, 5	RF_INP/RF_INN	RF differential input port
6	GND	radio-frequency zone
7	VCCHF	RF Crossover Analog Circuit 3.3V Power Port
9	VCCPS	RF Crossover Digital Circuit 3.3V Power Port
11	VCCPD	Phase Discriminator Module 3.3V Power Port
14	AVDD	Reference voltage 3.3V port
15	VPPCP	Charge Pump Module 3.3V Power Port
16	CP	Charge Pump Output Port
17	RVDD	Reference Crossover Module 3.3V Power Port
18	REF	Reference Signal Input Port
19	DVDD	LD, GPO module 3.3V power port
20	ASD	SPI auxiliary serial output port
21	VccDIG	Digital Module 3.3V Power Port
22	CEN	Chip enable port with internal integrated 80kΩ pull-up and 3.3/1.8V TTL level.
23	LE	SPI Serial to Parallel Conversion Control Signal, Rising Edge Trigger, Internal Integrated 80kΩ Pull Down, 3.3/1.8V TTL Levels
24	SDI	SPI serial data input, 3.3/1.8V TTL level.
8, 10, 12, 13	NC	vacant
DAP	GND	chip ground

Package Assembly Diagram



SP4 Dimension Table (unit:mm)			
Symbol	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.20Ref	
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D2	2.41	2.56	2.66
e		0.50BSC	
Ne		2.50BSC	
Nd		2.50BSC	
E	3.90	4.00	4.10
E2	2.41	2.56	2.66
K	0.20	---	---
L	0.30	0.40	0.50
aaa		0.08	

Description: 1. Unit: mm

2. Lead frame material: copper alloy

3. Package surface warpage: ≤0.05mm

4. All ground pins should be connected to PCB RF ground.

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SPI Control Description

I. Functional description

1. HMC mode and OPEN mode are supported;
2. Supports 3-wire write-only mode and 4-wire read/write mode; (SCK, LE,SDI,LD_GPO)
3. In HMC mode and OPEN mode, the register access address is 6 bits and the address range is 00h~3Fh; the register itself is 24 bits and the undefined part is treated as reserved bit;
4. Support for exception handling.

a) Read/write operation in HMC mode requires LE signal to be high all the time. If LE signal is pulled down during read/write operation, the read/write state machine enters the initial state and waits for the next read/write operation.

b) If a register with an undefined address is written, the slave ignores the operation;

c) To read a register with an undefined address or an undefined register bit, the slave defaults to returning a register value of all zeros

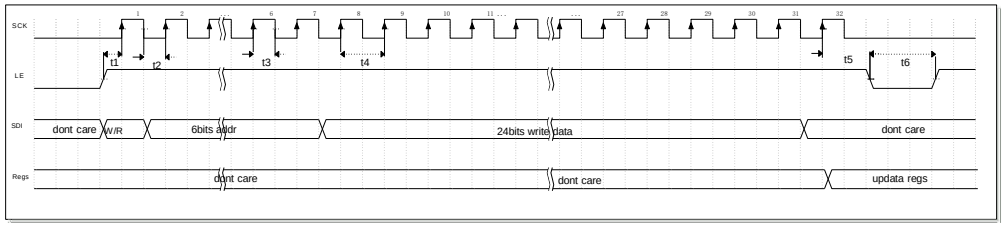
II. Timing Description

hmc model

hmc mode: the rising edge of LE appears before the rising edge of SCK.

hmc mode: 1 read/write control bit, 6bit address bit, 24bit data bit.

paradigm	parameters	descriptive	min	type	max	unit (of measure)
HMC	t1	LE rising edge to SCK establishment time		10		ns
	t2	SCK low level duration		10		ns
	t3	SCK high level duration		10		ns
	t4	SCK frequency		50		MHz
	t5	SCK rising edge to LE falling edge		15		ns
	t6	LE low level hold time		20		ns
OPEN	t1	SCK rising edge to LE establishment time		10		ns
	t2	SCK low level duration		10		ns
	t3	SDI Data Establishment Time		12		ns
	t4	SCK frequency		50		MHz
	t5	LE high level hold time		10		ns
	t6	SCK to LE lock data time		20		ns



Write Status.

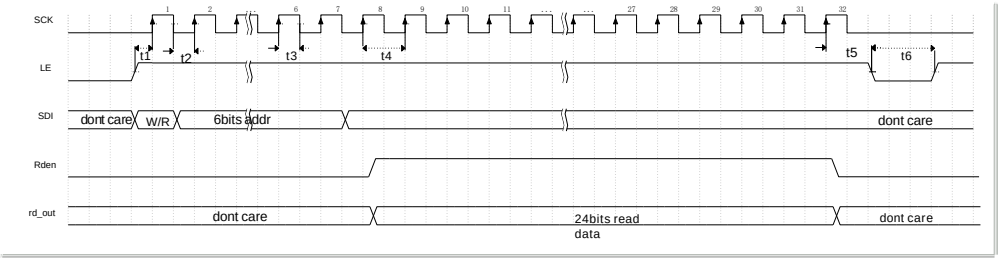
1: SCK first rising edge write read/write control bit; (1 SCK cycle)

2: SCK rising edge write 6 address bits, MSB priority; (2-7 SCK cycle)

3: SCK rising edge write 24-bit data, MSB priority; (8-31 SCK cycle)

4: The 32nd rising edge writes the data into the corresponding register; (32 SCK cycle)

5: After the minimum delay time t5, LE is cleared and a write cycle is completed.



SPI Control Description

Read state:

1: The first rising edge of SCK is written to the read/write control bit. (1 SCK cycle)

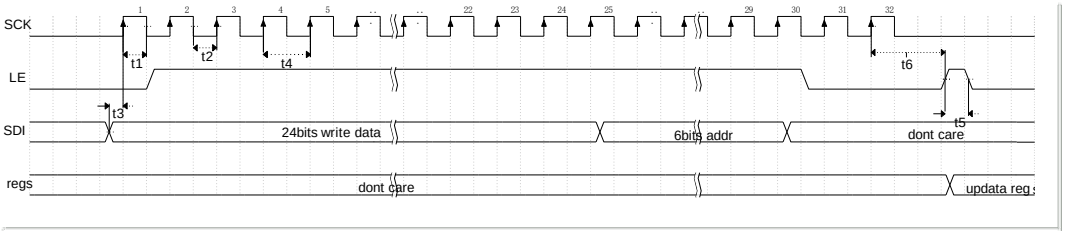
2: SCK rising edge writes 6 address bits. (2-7 SCK cycle)

3: SCK rising edge reads the value of the corresponding register (8-31 SCK cycle)

4: After a minimum delay时间t 5, the LE is cleared and a次写 cycle is completed. open mode

open mode: SCK rising edge appears before LE rising edge. open mode: 24bit data bit, 6bit address bit.

Write Status:



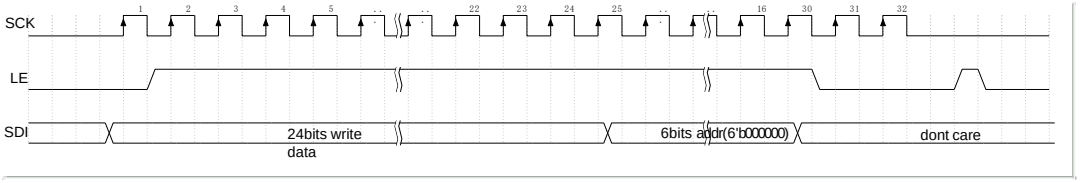
1: Write 24bit data on rising edge of SCK; (1-24 SCK cycle)

2: Write 6bit address on rising edge of SCK; (25-30 SCK cycle)

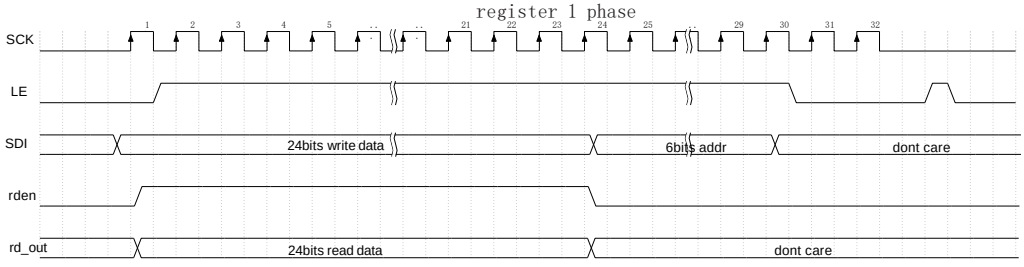
3: Set LE after the 32nd rising edge;

4: Update the corresponding register on the rising edge of LE.

Read state:



open read register 1 phase



open read register 2 phase

Phase I: Write register reg00 according to the write status of open mode; (address: 6'b000000). Phase II:

1: LE clear. Start the second cycle of read status;

2: The address of the first cycle according to the read state (data at the address shown in register 00h[5:0]) is placed on rd_out.

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SPI Control Description

III. Table of registers

name	address	christen	functionality	bit number bit	fill out or in (information on a form)	default value dfault-dec	descriptive
Read Address Register	00	read_addr e ss	Address for SPI read data	4:0	RW	0	Use only when SPI is open mode, write the address of the register to be read, read the data in the register corresponding to the address in LD_GPO.
Global Off Control Register	01	PD_ALL	Global shutdown control	0	RW	0	0: global normal operation 1: Global shutdown
		PD_REF	Switching Reference Channel	1	RW	0	1: Forced shutdown of the reference channel
		PD_RF	Switching Feedback Crossover	2	RW	0	1: Forced off feedback crossover
		PD_PFD	Switching frequency and phase detection PFD	3	RW	0	1: Forced PFD shutdown
		PD_CP	Switching Charge Pump CP	4	RW	0	1: Forced shutdown of charge pump
		PD_BIAS	Switching charge pump bias set current	5	RW	0	1: Forced shutdown of charge pump bias current
		PD_LD	Switch lock detection	6	RW	0	1: Forced shutdown lockout detection
		BLK_UVLO	Shielding of UVLO signals	7	RW	0	0: Disable undervoltage latch function at power-on reset 1: Enable undervoltage lockout
		RESET	reset register	8	RW	0	Reset all state machines and registers to default values. 0: Normal operation 1: Reset

SPI Control Description

name	address	christen	functionality	bit number bit	fill out or in (information on a form)	default value dfault-dec	description
Reference Frequency Division Register	02	rdiv	Reference Crossover Ratio	13:0	RW	1	Crossover ratio 1--16383 (2^14-1)
		Reserved	reserved bit	14	RW	0	reserved bit
		RST_REF	Reset Reference Crossover	15	RW	0	Reset Reference Divider, Highly Effective
		en_ref2div	Reference signal to number word enable (computing)	16	RW	1	Reference signal to digital enable, active high
Integer Frequency Division Register	03	intg	Feedback Crossover Ratio	14:0	RW	100	Integer mode: Crossover ratio 20~32767 (2^15-1)
		Reverse	reserved bit	20:15	RW	0	reserved bit
		pd_rst_div	Reset feedback crossover	21	RW	0	Reset feedback crossover, highly effective
fractional frequency register tool	04	frac	fractional crossover ratio	23:0	RW	100	Setting the fractional crossover ratio NUM[23:0]

SPI Control Description

name (of a person or thing)	address	christen	functionality	bit number bit	fill out or in (information on a form)	default value dfault-dec	descriptive
Fractional frequency division control register	06	n_reset_dsm	reset fractional crossover frequency	0	RW	1	Initial reset signal, low level reset
		dsm_en	Switched Fractional Crossover	1	RW	1	0: Fractional crossover frequency off 1: Turn on fractional crossover
		Reverse	reserved bit	3:2	RW	0	reserved bit
		mash2_en	The order of the mash pattern criticize (i.e. enumerate shortcomings)	4	RW	0	0: third-order mash 1: Second-order mash
		int_en	Switching Integer Mode	5	RW	0	0: Fractional mode 1: Integer mode (fractional crossover disabled)
		dither_en	Switch jitter	6	RW	0	0: no jitter 1: Self-jitter or LFSR jitter
		dith-er_type	LFSR jitter mode	7	RW	1	Valid only if dither_en=1: 0: LFSR jitter 1: Self-jittering
		mash_seed_en	mash initial state enable (sb. to do sth)	8	RW	0	0: Initial state is default value 0 1: Initial state can be set by mash_seed
		NDiv_Clk_to_dig_en	feedback divider to number Clock enable for word	9	RW	1	0: shutdown 1: Enabling
		NDiv_Clk_phase	feedback divider to number Word Clock Phase Control	10	RW	0	0: Same phase 1: Inverted phase
		Ndiv_Clk_delay	feedback divider to number Word clock delay control	12:11	RW	0	00: Delay 1 10: Delay 2 11: Delay 3

SPI Control Description

name (of a person or thing)	address	christen	functionality	bit number bit	fill out or in (information on a form)	default value dfault-dec	descriptive
Decimal frequency seedA	07	mash_seed	Fractional divider initial state	23:0	RW	0	mash_seed[23:0]
Latch Detect and Master Parallel Output Registers	09	LD_window	The digital LD determines the size of the window.	2:0	RW	0	The number LD determines the window size: 000: 2ns 001: 5.5ns 010: 11ns 011: 21ns 100: 30ns 101: 58ns 110: 114ns 111: 224ns
		LD_wincnt	Digital LD Window Determination Meter Value	4:3	RW	0	The LD is judged to be valid after the number of times the PFD is within the window reaches the set value: 00:64 01: 256 10: 1024 11:4096
		LD_MODE	LD operating mode	5	RW	0	LD operating mode: 0: Digital LD mode (PFD delay window mode) 1: Analog LD mode (PFD duty cycle mode)

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SPI Control Description

name (of a person or thing)	address	christen	functionality	bit number bit	fill out or in (information on a form)	default value dfault-dec	descriptive
lockout control measurements and surveys parallel port output leave sth. with sb. tool	09	Reverse	reserved bit	7:0	RW	0	reserved bit
		LD_DCC	Analog LD Duty Cycle Judgment Range	10:8	RW	0	LD Duty Cycle Determination Range: 000: 10% 001: 15% 010: 20% 011: 25% 100: 30% 101: 35% 110: 40% 111: 45%
		Reverse	reserved bit	15:11	RW	0	reserved bit
		GPO	global and port output	19:16	RW	0	Analog output selection for the LD_GPO_OUT pin output: 0000: NC not connected 0001: Reference divider REF_DIV 0010: Feedback divider RF_DIV 0011: Charge pump UP 0100: Charge pump DN 0101: Tuning voltage VCP_mir1 0110: Tuning voltage VCP_mir2 0111: Undervoltage lockout VUVLO 1000-1111: NC not connected The output of the LD_GPO_OUT pin is controlled by the RD_EN and GPO_EN, RD_EN is always high, LE(SEN) has step (low to high or high to low) then RD_EN is low. Selector The formula is as follows:

SPI Control Description

name (of a person or thing)	address	christen	functionality	bit number bit	fill out or in (information on a form)	default value dfault-dec	descriptive
							(low to high or high to low) then RD_EN is low. Selector The formula is as follows: When RD_EN=1 (high), LD_GPO_OUT=SDO (irrelevant) (GPO_EN high or low); When RD_EN=0 (low) and GPO_EN=0, the LD_GPO_OUT=LD; When RD_EN=0 (low) and GPO_EN=1, the LD_GPO_OUT = analog output (see above)
		Reverse	reserved bit	22:20	RW	0	reserved bit
		GPO_EN	Switch GPO	23	RW	0	0: Turn off GPO in LD mode 1: Shutdown LD with GPO mode

SPI Control Description

name (of a person or thing)	address	christen	functionality	bit number bit	fill out or in (information on a form)	default value dfault-dec	descriptive
frequency sharing forensics The charge of the device and the charge of the pump Depository A	10	PD_tdelay	Set PFD reset delay time	1:0	RW	0	PFD reset delay: 00: 0.6ns 01: 1ns 10: 1.4ns 11: 1.8ns
		POL_INV	Setting PFD polarity	2	RW	1	PFD polarity control: 0: Positive polarity 1: Reverse polarity
		Reverse	reserved bit	4:3	RW	0	reserved bit
		FUP_CP	Forces the UP output of the PFD to be enabled.	5	RW	0	Effective only with PFD off 0: Force the UP output of the PFD to be turned off 1: Force the UP output of the PFD to be enabled
		FDN_CP	Forces the DN output of the PFD to be enabled.	6	RW	0	Effective only with PFD off 0: Forced shutdown of the DN output of the PFD 1: Forces the DN output of the PFD to be enabled
		Reverse	reserved bit	7	RW	0	reserved bit
		CPGup	CP gain current UP control word	15:8	RW	255	CP gain current UP control word (30uA/bit): Current calculation: 30uA*CPGup CPGup range: 0-255
		CPGdn	CP gain current DN control word	23:16	RW	255	CP gain current DN control word (30uA/bit): Current calculation: 30uA*CPGdn CPGdn range: 0-255

Frequency and phase discriminators and charge pumps are sent to a single source. Depository B	11	CPOS_current	CP Compensation Current Control Word	6:0	RW	0	CP compensation current DN control word (7.5uA/bit): Current calculation: 7.5uA*CPOS_current CPOS_current range: 0-127
		Reverse	reserved bit	7	RW	0	reserved bit
		CPOS_UP_EN	UP Compensation current for switching CP	8	RW	0	0: UP compensation current for turning off the CP 1: Turn on the UP compensation current of the CP
		CPOS_DN_EN	DN of switching CP Compensation current	9	RW	0	0: UP compensation current for turning off the CP 1: Turn on the UP compensation current of the CP
		reserved	reserved bit	10	RW	0	
		Ndiv BIAS	Feedback crossover current regulation	13:11	RW	2	000: Minimum current 001: Current + 5% 010: Current + 10%

evaluation board

Evaluation Board Model	VCO Model	VCO Frequency Range
EVAL-CWPL219SP4-A	CWV022SP4 (single segment)	10~20GHz
EVAL-CWPL219SP4-C	CWV100SP4 (segmented)	10~20GHz
EVAL-CWPL219SP4-D	CWV008SP4	19.5~22.5GHz
EVAL-CWPL219SP4-E	SV5510SP4	9.44~10.30GHz

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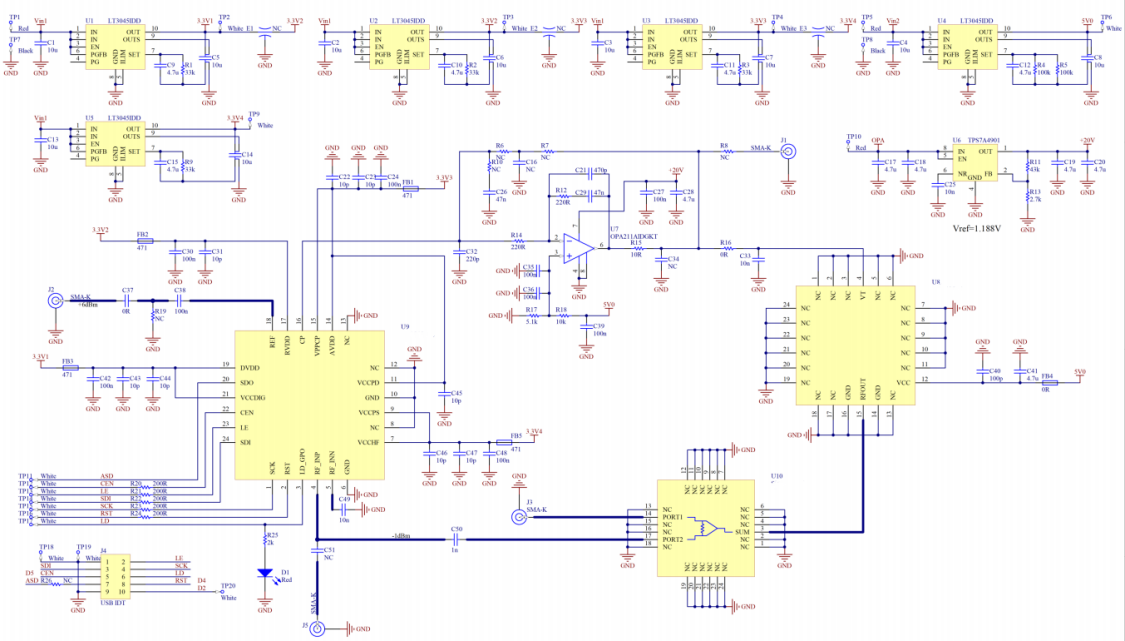
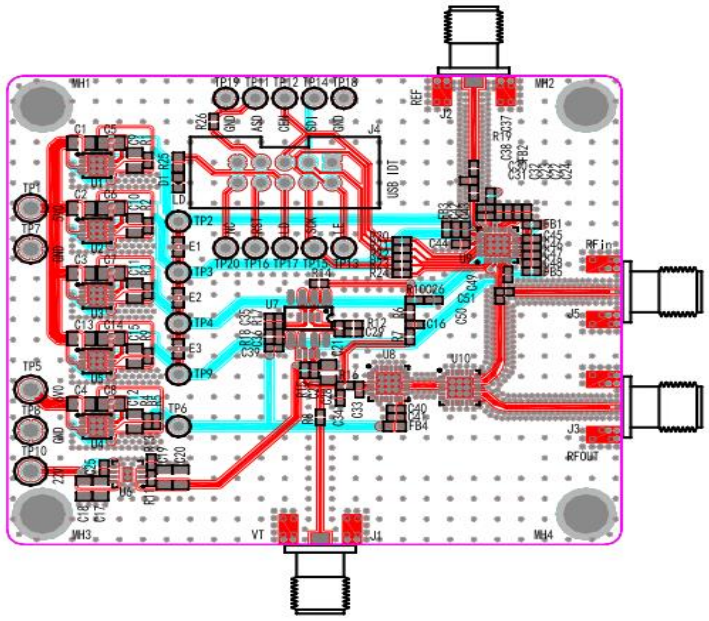
Website: www.cdcwtec.com

Evaluation Board Circuit Diagram (EVAL-CWPL219SP4-A)

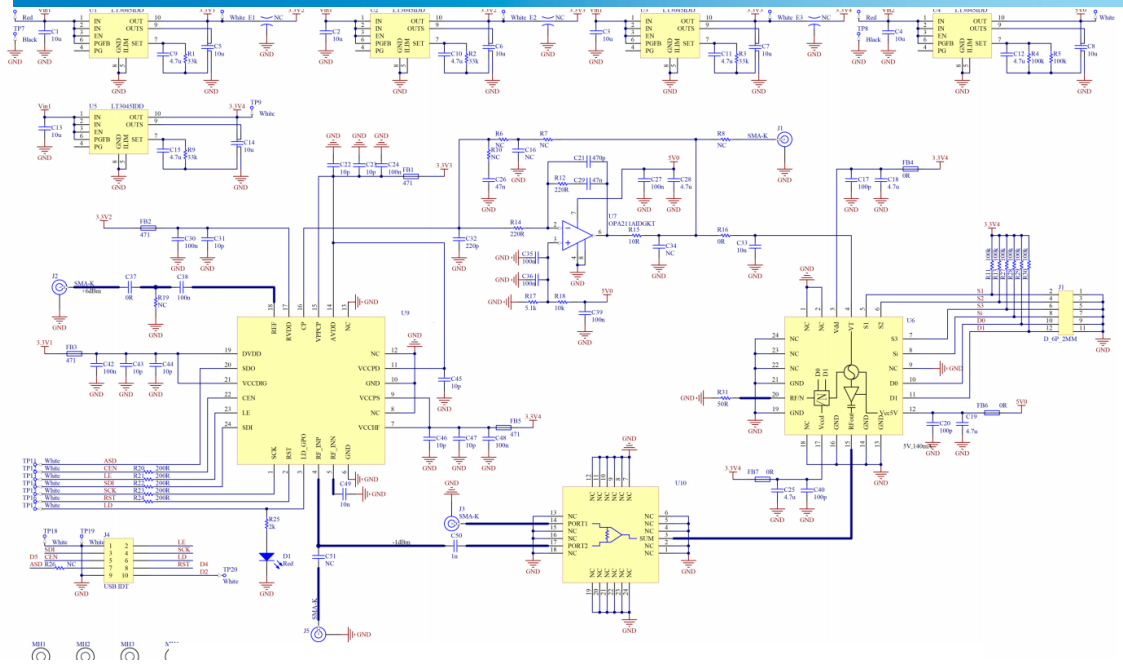


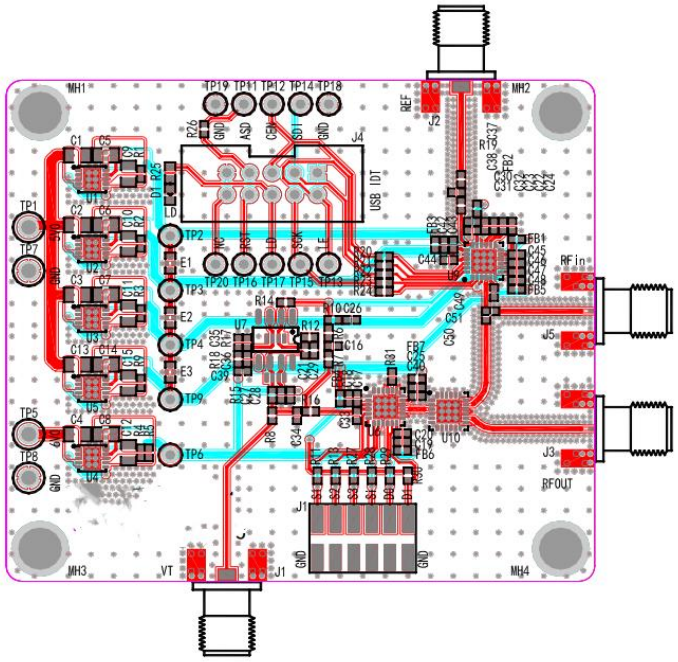


Evaluation Board Circuit Diagram (EVAL-CWPL219SP4-A)

#	Designator	Comment	Description	Footprint	Manufacturer	Part Number	SOB	Quantity
1	!PCB1	PCB	Printed Circuit Board		Si_Core	EVAL-SIPL6SP4-A	Y	1
2	C1, C2, C3, C4, C5, C6, C7, C8, C13, C14	10u	Capacitor	0805, 0805_4	TDK	C2012X5R1E106K125AB	Y	10
3	C9, C10, C11, C12, C15, C17, C18, C19, C20, C28	4.7u	Capacitor	0805	TDK	C2012X5R1E475K125AB	Y	10
4	C16	NC	Capacitor	0402	Murata	GRM155R71H104KE14D	N	1
5	C21	470p	Capacitor	0402	Murata	GCM1555C1H471JA16D	Y	1
6	C22, C23, C31, C43, C44, C45, C46, C47	10p	Capacitor	0402	Murata	GRM1555C1H100FA01D	Y	8
7	C24, C27, C30, C35, C36, C38, C39, C42, C48	100n	Capacitor	0402	Murata	GRM155R71H104KE14D	Y	9
8	C25, C33, C49	10n	Capacitor	0402	Murata	GRM155R71H103JA88D	Y	3
9	C26	47n	Capacitor	0402	Murata	GRM155R71C473KA01D	Y	1
10	C29	47n	Capacitor	0402	Murata	GRM155R71E473JA88D	Y	1
11	C32	220p	Capacitor	0402	Murata	GCM155R71H221JA37D	Y	1
12	C34	NC	Capacitor	0402	Murata	GCM155R71H222JA37D	Y	1
13	C37, R16	0R	Capacitor, Resistor	0402	Yageo	RC0402JR-070RL	Y	2
14	C40	100p	Capacitor	0402	Murata	GRM1555C1H101FA01D	Y	1
15	C41	4.7u	Capacitor	0402	TDK	C1005X5R1A475K050BC	Y	1
16	C50	1n	Capacitor	0402	Murata	GRM1555C1H102JA01D	Y	1
17	C51	NC	Capacitor	0402	Murata	GRM1555C1H102JA01D	N	1
18	D1	Red	LED	0603D	WE	150060SS75003	Y	1
19	E1, E2, E3	NC	EMI Filter	NFM18C	Murata	NFM18CC223R1C3	N	3
20	FB1, FB2, FB3, FB5	471	470R	0402	Murata	BLM15BD471SH1	Y	4
21	FB4	0R	Resistor	0603	Yageo	RC0603JR-070RL	Y	1
22	J1, J2, J3, J5	SMA-K	RF Connecter	SMA_40G, SMA_DC	傲文	D550B12E01-023	Y	4
23	J4	USB IDT	Header, 5-Pin, Dual row	IDC2.54-10		DC3-10P	Y	1
24	MH1, MH2, MH3, MH4	702932000		702932000	WE	702932000	Y	4
25	R1, R2, R3, R9	33k	Resistor	0402	Yageo	RC0402FR-0733KL	Y	4
26	R4, R5	100k	Resistor	0402	Yageo	RC0402FR-07100KL	Y	2
27	R6	NC	Resistor	0402	Yageo	RC0402FR-07750RL	N	1
28	R7, R8, R26	NC	Resistor	0402	Yageo	RC0402JR-070RL	N	3
29	R10	NC	Resistor	0402	Yageo	RC0402FR-07300RL	N	1
30	R11	43k	Resistor	0402		RC0402FR-0743KL	Y	1
31	R12, R14	220R	Resistor	0402	Yageo	RC0402JR-07220RL	Y	2
32	R13	2.7k	Resistor	0402		RC0402FR-072K7L	Y	1
33	R15	10R	Resistor	0402	Yageo	RC0402JR-0710RL	Y	1
34	R17	5.1k	Resistor	0402	Yageo	RC0402FR-075K1L	Y	1
35	R18	10k	Resistor	0402	Yageo	RC0402FR-0710KL	Y	1
36	R19	NC	Resistor	0402	Yageo	RC0402FR-07100RL	N	1
37	R20, R21, R22, R23, R24	200R	Resistor	0402	Yageo	RC0402FR-07200RL	N	5
38	R25	2k	Resistor	0603	Yageo	RC0603FR-072KL	Y	1
39	TP1, TP5, TP10	Red	Test Point	Keystone5005	Keystone	Keystone5005	Y	3
40	TP2, TP3, TP4, TP6, TP9	White	Test Point	Keystone5002	Keystone	Keystone5002	N	5
41	TP7, TP8	Black	Test Point	Keystone5006	Keystone	Keystone5006	Y	2
42	TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20	White	Test Point	Keystone5002	Keystone	Keystone5002	Y	10
43	U1, U2, U3, U4, U5	LT3045IDD	LDO	DFN10	ADI	LT3045IDD	Y	5
44	U6	TPS7A4901	PLDO for RF, 150mA output	SON-8	TI	TPS7A4901DRBR	Y	1
45	U7	OPA211AIDGKT	Operational Amplifier	SOP8-1	TI	OPA211AIDGKR	Y	1
46	U8	SIV022SP4	VCO	SP4	Si_Core	SIV022SP4	Y	1
47	U9	SIPL219SP4	PLL	SP4	Si_Core	SIPL219SP4	Y	1
48	U10	SIPS121SP4	Power Splitter/Combiner	SP4	Si_Core	SIPS121SP4	Y	1

Evaluation Board Circuit Diagram (EVAL-CWPL219SP4-C)

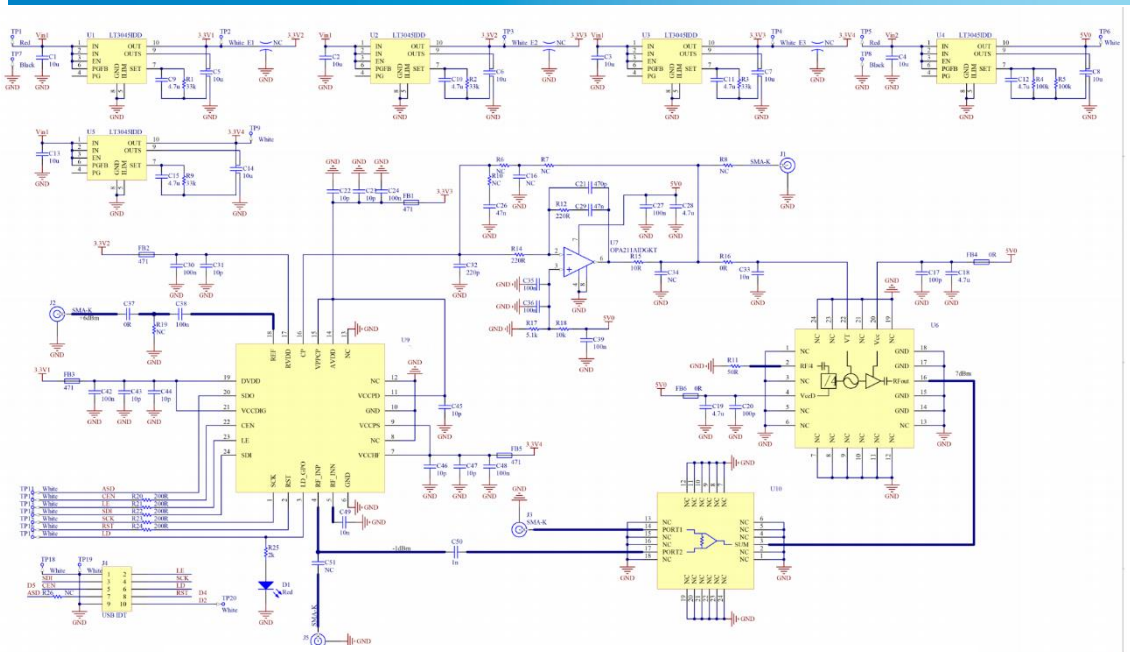


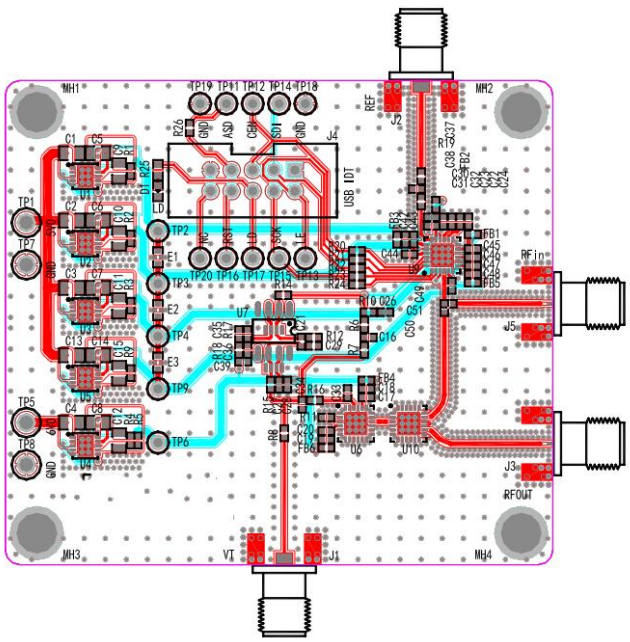


Evaluation Board Circuit Diagram (EVAL-CWPL219SP4-C

#	Designator	Comment	Description	Footprint	Manufacturer	Part Number	SOB	Quantity
1	!PCB1	PCB	Printed Circuit Board		Si_Core	EVAL-SIPL6SP4-C	Y	1
2	C1, C2, C3, C4, C5, C6, C7, C8, C13, C14	10u	Capacitor	0805, 0805_4	TDK	C2012X5R1E106K125AB	Y	10
3	C9, C10, C11, C12, C15	4.7u	Capacitor	0805	TDK	C2012X5R1E475K125AB	Y	5
4	C16	NC	Capacitor	0402	Murata	GRM155R71H104KE14D	N	1
5	C17, C20, C40	100p	Capacitor	0402	Murata	GRM1555C1H101FA01D	Y	3
6	C18, C19, C25, C28	4.7u	Capacitor	0402	TDK	C1005X5R1A475K050BC	Y	4
7	C21	470p	Capacitor	0402	Murata	GCM1555C1H471JA16D	Y	1
8	C22, C23, C31, C43, C44, C45, C46, C47	10p	Capacitor	0402	Murata	GRM1555C1H100FA01D	Y	8
9	C24, C27, C30, C35, C36, C38, C39, C42, C48	100n	Capacitor	0402	Murata	GRM155R71H104KE14D	Y	9
10	C26	47n	Capacitor	0402	Murata	GRM155R71C473KA01D	Y	1
11	C29	47n	Capacitor	0402	Murata	GRM155R71E473JA88D	Y	1
12	C32	220p	Capacitor	0402	Murata	GCM155R71H221JA37D	Y	1
13	C33, C49	10n	Capacitor	0402	Murata	GRM155R71H103JA88D	Y	2
14	C34	NC	Capacitor	0402	Murata	GCM155R71H222JA37D	Y	1
15	C37, FB4, FB6, FB7, R16	0R	Capacitor, Resistor	0402	Yageo	RC0402JR-070RL	Y	5
16	C50	1n	Capacitor	0402	Murata	GRM1555C1H102JA01D	Y	1
17	C51	NC	Capacitor	0402	Murata	GRM1555C1H102JA01D	N	1
18	D1	Red	LED	0603D	WE	150060SS75003	Y	1
19	E1, E2, E3	NC	EMI Filter	NFM18C	Murata	NFM18CC223R1C3	N	3
20	FB1, FB2, FB3, FB5	471	470R	0402	Murata	BLM15BD471SH1	Y	4
21	J1	D_6P_2MM	HEADER	D_6P_2MM	Harwin	M22-5320605	Y	1
22	J1, J2, J3, J5	SMA-K	RF Connecter	SMA_40G, SMA_DC	傲文	D550B12E01-023	Y	4
23	J4	USB IDT	Header, 5-Pin, Dual row	IDC2.54-10		DC3-10P	Y	1
24	MH1, MH2, MH3, MH4	702932000		702932000	WE	702932000	Y	4
25	R1, R2, R3, R9	33k	Resistor	0402	Yageo	RC0402FR-0733KL	Y	4
26	R4, R5, R11, R13, R27, R28, R29, R30	100k	Resistor	0402	Yageo	RC0402FR-07100KL	Y	8
27	R6	NC	Resistor	0402	Yageo	RC0402FR-07750RL	N	1
28	R7, R8, R26	NC	Resistor	0402	Yageo	RC0402JR-070RL	N	3
29	R10	NC	Resistor	0402	Yageo	RC0402FR-07300RL	N	1
30	R12, R14	220R	Resistor	0402	Yageo	RC0402JR-07220RL	Y	2
31	R15	10R	Resistor	0402	Yageo	RC0402JR-0710RL	Y	1
32	R17	5.1k	Resistor	0402	Yageo	RC0402FR-075K1L	Y	1
33	R18	10k	Resistor	0402	Yageo	RC0402FR-0710KL	Y	1
34	R19	NC	Resistor	0402	Yageo	RC0402FR-07100RL	N	1
35	R20, R21, R22, R23, R24	200R	Resistor	0402	Yageo	RC0402FR-07200RL	N	5
36	R25	2k	Resistor	0603	Yageo	RC0603FR-072KL	Y	1
37	R31	50R	Resistor	0402	Yageo	RC0402JR-0750RL	Y	1
38	TP1, TP5	Red	Test Point	Keystone5005	Keystone	Keystone5005	Y	2
39	TP2, TP3, TP4, TP6, TP9	White	Test Point	Keystone5002	Keystone	Keystone5002	N	5
40	TP7, TP8	Black	Test Point	Keystone5006	Keystone	Keystone5006	Y	2
41	TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20	White	Test Point	Keystone5002	Keystone	Keystone5002	Y	10
42	U1, U2, U3, U4, U5	LT3045IDD	LDO	DFN10	ADI	LT3045IDD	Y	5
43	U6	SIV100SP4	VCO	SP4	Si_Core	SIV100SP4	Y	1
44	U7	OPA211AIDGKT	Operational Amplifier	SOP8-1	TI	OPA211AIDGKR	Y	1
45	U9	SIPL219SP4	PLL	SP4	Si_Core	SIPL219SP4	Y	1
46	U10	SIPS121SP4	Power Splitter/Combiner	SP4	Si_Core	SIPS121SP4	Y	1

Evaluation Board Circuit Diagram (EVAL-CWPL219SP4-D)

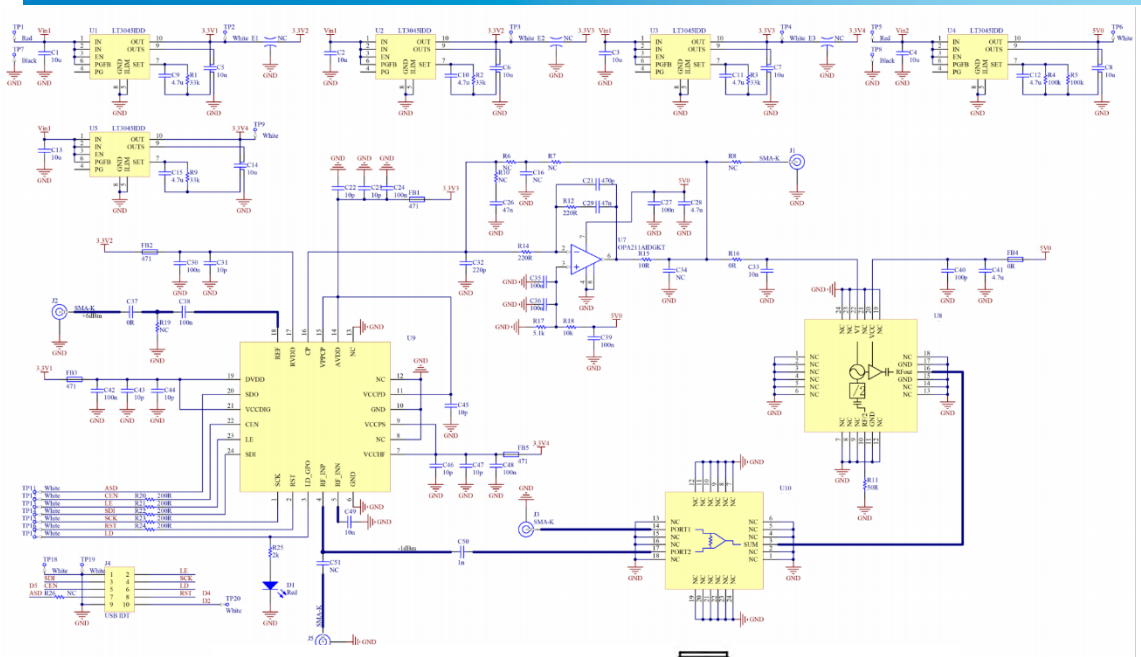


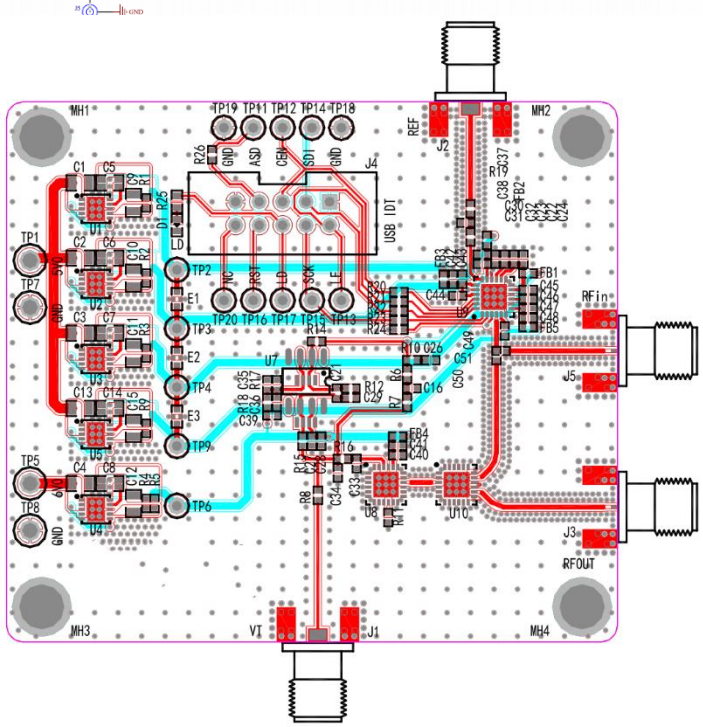


Evaluation Board Circuit Diagram (EVAL-CWPL219SP4-D

#	Designator	Comment	Description	Footprint	Manufacturer	Part Number	SOB	Quantity
1	!PCB1	PCB	Printed Circuit Board		Si_Core	EVAL-SIPL6SP4-E	Y	1
2	C1, C2, C3, C4, C5, C6, C7, C8, C13, C14	10u	Capacitor	0805, 0805_4	TDK	C2012X5R1E106K125AB	Y	10
3	C9, C10, C11, C12, C15	4.7u	Capacitor	0805	TDK	C2012X5R1E475K125AB	Y	5
4	C16	NC	Capacitor	0402	Murata	GRM155R71H104KE14D	N	1
5	C17, C20	100p	Capacitor	0402	Murata	GRM1555C1H101FA01D	Y	2
6	C18, C19, C28	4.7u	Capacitor	0402		C1005X5R1A475K050BC	Y	3
7	C21	470p	Capacitor	0402	Murata	GCM1555C1H471JA16D	Y	1
8	C22, C23, C31, C43, C44, C45, C46, C47	10p	Capacitor	0402	Murata	GRM1555C1H100FA01D	Y	8
9	C24, C27, C30, C35, C36, C38, C39, C42, C48	100n	Capacitor	0402	Murata	GRM155R71H104KE14D	Y	9
10	C26	47n	Capacitor	0402	Murata	GRM155R71C473KA01D	Y	1
11	C29	47n	Capacitor	0402	Murata	GRM155R71E473JA88D	Y	1
12	C32	220p	Capacitor	0402	Murata	GCM155R71H221JA37D	Y	1
13	C33, C49	10n	Capacitor	0402	Murata	GRM155R71H103JA88D	Y	2
14	C34	NC	Capacitor	0402	Murata	GCM155R71H222JA37D	Y	1
15	C37, FB4, FB6, R16	0R	Capacitor, Resistor	0402	Yageo	RC0402JR-070RL	Y	4
16	C50	1n	Capacitor	0402	Murata	GRM1555C1H102JA01D	Y	1
17	C51	NC	Capacitor	0402	Murata	GRM1555C1H102JA01D	N	1
18	D1	Red	LED	0603D	WE	150060SS75003	Y	1
19	E1, E2, E3	NC	EMI Filter	NFM18C	Murata	NFM18CC223R1C3	N	3
20	FB1, FB2, FB3, FB5	471	470R	0402	Murata	BLM15BD471SH1	Y	4
21	J1, J2, J3, J5	SMA-K	RF Connecter	SMA_40G, SMA_DC	傲文	D550B12E01-023	Y	4
22	J4	USB IDT	Header, 5-Pin, Dual row	IDC2.54-10		DC3-10P	Y	1
23	MH1, MH2, MH3, MH4	702932000		702932000	WE	702932000	Y	4
24	R1, R2, R3, R9	33k	Resistor	0402	Yageo	RC0402FR-0733KL	Y	4
25	R4, R5	100k	Resistor	0402	Yageo	RC0402FR-07100KL	Y	2
26	R6	NC	Resistor	0402	Yageo	RC0402FR-07750RL	N	1
27	R7, R8, R26	NC	Resistor	0402	Yageo	RC0402JR-070RL	N	3
28	R10	NC	Resistor	0402	Yageo	RC0402FR-07300RL	N	1
29	R11	50R	Resistor	0402	Yageo	RC0402JR-0750RL	Y	1
30	R12, R14	220R	Resistor	0402	Yageo	RC0402JR-07220RL	Y	2
31	R15	10R	Resistor	0402	Yageo	RC0402JR-0710RL	Y	1
32	R17	5.1k	Resistor	0402	Yageo	RC0402FR-075K1L	Y	1
33	R18	10k	Resistor	0402	Yageo	RC0402FR-0710KL	Y	1
34	R19	NC	Resistor	0402	Yageo	RC0402FR-07100RL	N	1
35	R20, R21, R22, R23, R24	200R	Resistor	0402	Yageo	RC0402FR-07200RL	N	5
36	R25	2k	Resistor	0603	Yageo	RC0603FR-072KL	Y	1
37	TP1, TP5	Red	Test Point	Keystone5005	Keystone	Keystone5005	Y	2
38	TP2, TP3, TP4, TP6, TP9	White	Test Point	Keystone5002	Keystone	Keystone5002	N	5
39	TP7, TP8	Black	Test Point	Keystone5006	Keystone	Keystone5006	Y	2
40	TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20	White	Test Point	Keystone5002	Keystone	Keystone5002	Y	10
41	U1, U2, U3, U4, U5	LT3045IDD	LDO	DFN10	ADI	LT3045IDD	Y	5
42	U6	SIV008SP4	VCO	SP4	Si_Core	SIV008SP4	Y	1
43	U7	OPA211AIDGKT	Operational Amplifier	SOP8-1	TI	OPA211AIDGKR	Y	1
44	U9	SIPL219SP4	PLL	SP4	Si_Core	SIPL219SP4	Y	1
45	U10	SIPS121SP4	Power Splitter/Combiner	SP4	Si_Core	SIPS121SP4	Y	1

Evaluation Board Circuit Diagram (EVAL-CWPL219SP4-E)





Evaluation Board Circuit Diagram (EVAL-CWPL219SP4-E

#	Designator	Comment	Description	Footprint	Manufacturer	Part Number	SOB	Quantity
1	!PCB1	PCB	Printed Circuit Board		Si_Core	EVAL-SIPL6SP4-D	Y	1
2	C1, C2, C3, C4, C5, C6, C7, C8, C13, C14	10u	Capacitor	0805, 0805_4	TDK	C2012X5R1E106K125AB	Y	10
3	C9, C10, C11, C12, C15	4.7u	Capacitor	0805	TDK	C2012X5R1E475K125AB	Y	5
4	C16	NC	Capacitor	0402	Murata	GRM155R71H104KE14D	N	1
5	C21	470p	Capacitor	0402	Murata	GCM1555C1H471JA16D	Y	1
6	C22, C23, C31, C43, C44, C45, C46, C47	10p	Capacitor	0402	Murata	GRM1555C1H100FA01D	Y	8
7	C24, C27, C30, C35, C36, C38, C39, C42, C48	100n	Capacitor	0402	Murata	GRM155R71H104KE14D	Y	9
8	C26	47n	Capacitor	0402	Murata	GRM155R71C473KA01D	Y	1
9	C28, C41	4.7u	Capacitor	0402	TDK	C1005X5R1A475K050BC	Y	2
10	C29	47n	Capacitor	0402	Murata	GRM155R71E473JA88D	Y	1
11	C32	220p	Capacitor	0402	Murata	GCM155R71H221JA37D	Y	1
12	C33, C49	10n	Capacitor	0402	Murata	GRM155R71H103JA88D	Y	2
13	C34	NC	Capacitor	0402	Murata	GCM155R71H222JA37D	Y	1
14	C37, FB4, R16	0R	Capacitor, Resistor	0402	Yageo	RC0402JR-070RL	Y	3
15	C40	100p	Capacitor	0402	Murata	GRM1555C1H101FA01D	Y	1
16	C50	1n	Capacitor	0402	Murata	GRM1555C1H102JA01D	Y	1
17	C51	NC	Capacitor	0402	Murata	GRM1555C1H102JA01D	N	1
18	D1	Red	LED	0603D	WE	150060SS75003	Y	1
19	E1, E2, E3	NC	EMI Filter	NFM18C	Murata	NFM18CC223R1C3	N	3
20	FB1, FB2, FB3, FB5	471	470R	0402	Murata	BLM15BD471SH1	Y	4
21	J1, J2, J3, J5	SMA-K	RF Connecter	SMA_40G, SMA_DC	傲文	D550B12E01-023	Y	4
22	J4	USB IDT	Header, 5-Pin, Dual row	IDC2.54-10		DC3-10P	Y	1
23	MH1, MH2, MH3, MH4	702932000		702932000	WE	702932000	Y	4
24	R1, R2, R3, R9	33k	Resistor	0402	Yageo	RC0402FR-0733KL	Y	4
25	R4, R5	100k	Resistor	0402	Yageo	RC0402FR-07100KL	Y	2
26	R6	NC	Resistor	0402	Yageo	RC0402FR-07750RL	N	1
27	R7, R8, R26	NC	Resistor	0402	Yageo	RC0402JR-070RL	N	3
28	R10	NC	Resistor	0402	Yageo	RC0402FR-07300RL	N	1
29	R11	50R	Resistor	0402	Yageo	RC0402JR-0750RL	Y	1
30	R12, R14	220R	Resistor	0402	Yageo	RC0402JR-07220RL	Y	2
31	R15	10R	Resistor	0402	Yageo	RC0402JR-0710RL	Y	1
32	R17	5.1k	Resistor	0402	Yageo	RC0402FR-075K1L	Y	1
33	R18	10k	Resistor	0402	Yageo	RC0402FR-0710KL	Y	1
34	R19	NC	Resistor	0402	Yageo	RC0402FR-07100RL	N	1
35	R20, R21, R22, R23, R24	200R	Resistor	0402	Yageo	RC0402FR-07200RL	N	5
36	R25	2k	Resistor	0603	Yageo	RC0603FR-072KL	Y	1
37	TP1, TP5	Red	Test Point	Keystone5005	Keystone	Keystone5005	Y	2
38	TP2, TP3, TP4, TP6, TP9	White	Test Point	Keystone5002	Keystone	Keystone5002	N	5
39	TP7, TP8	Black	Test Point	Keystone5006	Keystone	Keystone5006	Y	2
40	TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20	White	Test Point	Keystone5002	Keystone	Keystone5002	Y	10
41	U1, U2, U3, U4, U5	LT3045IDD	LDO	DFN10	ADI	LT3045IDD	Y	5
42	U7	OPA211AIDGKT	Operational Amplifier	SOP8-1	TI	OPA211AIDGKR	Y	1
43	U8	SV5510SP4	VCO	SP4	Si_Core	SV5510SP4	Y	1
44	U9	SIPL219SP4	PLL	SP4	Si_Core	SIPL219SP4	Y	1
45	U10	SIPS121SP4	Power Splitter/Combiner	SP4	Si_Core	SIPS121SP4	Y	1