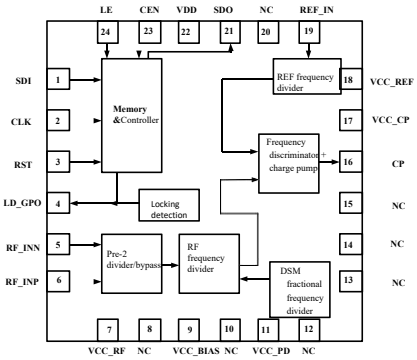
Performance characteristics

- RF Input Frequency Range of DC ~ 15GHz
- Internally integrated 19-bit continuous programmable frequency divider
- Normalized floor noise:
  Decimal mode:-223dBc/Hz Integer mode:-224dBc/Hz
- Phase discrimination frequency exceeding 100MHz
- 3.3 V power supply
- Packaging form of QFN24 4*4

Typical application

- Satellite communication system
- Point-to-point radio

Functional block diagram



Overview

CWPL491SP4 is a fractional phase-locked loop packaged in 4*4mm QFN24;; The VCO divider with low phase noise, reference divider, phase detector and phase locked loop module with precise gain control are integrated internally.

Phase-locked loop fractional frequency division can support 24 bits, SPI can support general open mode and integrate data read-back function.

Electrical performance table (TA=25 ℃, VDD=3. 3V)

Test parameters	Describe	Unit	Indicator parameter		
			Minimum value	Typical value	Maximum value
REF parameter					
REF frequency range	Input sine wave	MHz	16		500
Input power range		dBm	-5		11
Phase discrimination frequency range	Decimal pattern	MHz	16		125
	Integer mode	MHz	16		150
R Divider Ratio			1		16383
RF parameter					
RF frequency range	Turn on the front frequency division of 2	GHz	1.3		15
	Turn off the front frequency division 2	GHz	0.5		5
Radio frequency feedback power	Turn on the front frequency division of 2	dBm	-15		15
	Turn off the front frequency division 2	dBm	-15		15
N-division ratio	Turn on the front frequency division of 2		32		1048574
	Turn off the front frequency division 2		16		524287
Fractional frequency division ratio	Turn on the front frequency division of 2		40		1048566
Charge pump parameters					
Minimum CP current		mA		0.43	
Maximum CP current		mA		5.15	
CP leakage current		mA		TBD	
Basic functional parameters					
Supply current	3.3 V	mA		123	
Turn-off current		mA		19.3	

Electrical performance table (TA=25 ℃, VDD=3. 3V) (continued)

Test parameters		Describe	Unit	Indicator parameter		
				Minimum value	Typical value	Maximum value
PLL closed-loop parameters						
Normalized floor noise		Integer mode, PD=100MHz, VCO=10GHz	dBc/Hz		-224	
		Decimal mode, PD=100MHz, VCO=10. 001 GHz	dBc/Hz		-223	
Phase noise	Phase Noise @ 100Hz	fin=100MHz, Pin=5dBm, VCO=2GHz	dBc/Hz		-96	
	Phase Noise @ 1kHz		dBc/Hz		-106	
	Phase Noise @ 10kHz		dBc/Hz		-114	
	Phase Noise @ 100kHz		dBc/Hz		-117	
	Phase Noise @ 1MHz		dBc/Hz		-132	
	Phase Noise @ 10MHz		dBc/Hz		-152	
Phase noise	Phase Noise @ 100Hz	fin=100MHz, Pin=5dBm, VCO=5GHz	dBc/Hz		-88	
	Phase Noise @ 1kHz		dBc/Hz		-99	
	Phase Noise @ 10kHz		dBc/Hz		-107	
	Phase Noise @ 100kHz		dBc/Hz		-111	
	Phase Noise @ 1MHz		dBc/Hz		-126	
	Phase Noise @ 10MHz		dBc/Hz		-147	
Phase noise	Phase Noise @ 100Hz	fin=100MHz, Pin=5dBm, VCO=10GHz	dBc/Hz		-82	
	Phase Noise @ 1kHz		dBc/Hz		-92	
	Phase Noise @ 10kHz		dBc/Hz		-101	
	Phase Noise @ 100kHz		dBc/Hz		-104	
	Phase Noise @ 1MHz		dBc/Hz		-122	
	Phase Noise @ 10MHz		dBc/Hz		-140	
Phase noise	Phase Noise @ 100Hz	fin=100MHz, Pin=5dBm, VCO=10. 001 GHz	dBc/Hz		-81	
	Phase Noise @ 1kHz		dBc/Hz		91	
	Phase Noise @ 10kHz		dBc/Hz		-99	
	Phase Noise @ 100kHz		dBc/Hz		-103	
	Phase Noise @ 1MHz		dBc/Hz		-118	
	Phase Noise @ 10MHz		dBc/Hz		-139	
Phase noise	Phase Noise @ 100Hz	fin=100MHz, Pin=5dBm, VCO=5. 001 GHz	dBc/Hz		-85	
	Phase Noise @ 1kHz		dBc/Hz		-97	
	Phase Noise @ 10kHz		dBc/Hz		-105	
	Phase Noise @ 100kHz		dBc/Hz		-109	
	Phase Noise @ 1MHz		dBc/Hz		-120	
	Phase Noise @ 10MHz		dBc/Hz		-145	
Phase noise	Phase Noise @ 100Hz	fin=100MHz, Pin=5dBm, VCO=14GHz	dBc/Hz		-77	
	Phase Noise @ 1kHz		dBc/Hz		-87	
	Phase Noise @ 10kHz		dBc/Hz		-96	
	Phase Noise @ 100kHz		dBc/Hz		-101	
	Phase Noise @ 1MHz		dBc/Hz		-113	
	Phase Noise @ 10MHz		dBc/Hz		-137	
Spurious	Integer boundary spurious	REF=100MHz, RF=10. 001 GHz	dBc/Hz		TBD	
Lock detection function					Pull high after locking	

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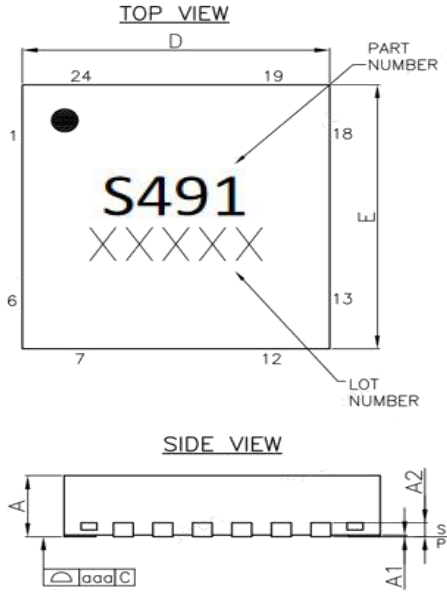
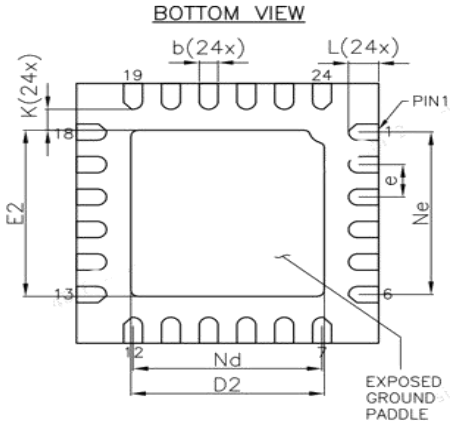
Address: No. 5, Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

Absolute maximum

Parameter	Scope
VDD	-0.3 V ~ 3.6 V
IO	-0.3 V ~ VDD+0. 3V
Operating temperature	-40 ℃ ~ 85 ℃
Storage temperature	-65 ℃ ~ 150 ℃
ESD-HBM	TBD

Chip package outline diagram

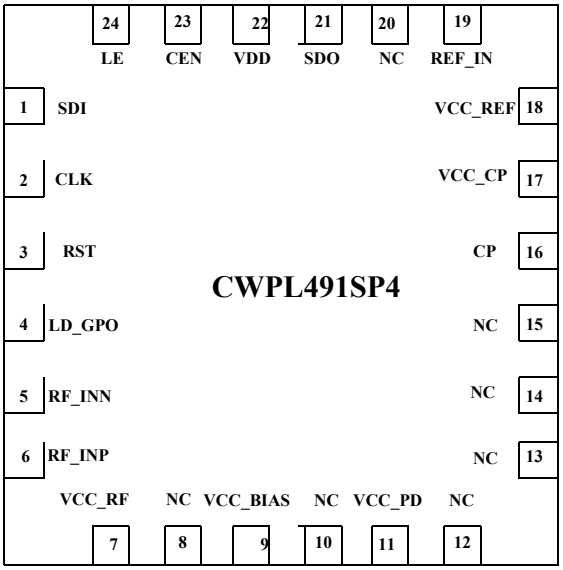




SP4 Dimension Table (unit:mm)			
Symbol	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.20Ref	
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D2	2.41	2.56	2.66
e		0.50BSC	
Ne		2.50BSC	
Nd		2.50BSC	
E	3.90	4.00	4.10
E2	2.41	2.56	2.66
K	0.20	---	---
L	0.30	0.40	0.50
aaa		0.08	

Description: 1. Unit mm
2. Lead frame material: copper alloy
3. Package surface warpage: ≤ 0. 05mm
4. Please connect all ground pins to PCB RF ground

Definition of pad



Pad description

PAD number	Name	Describe
1	SDI	SPI Serial Data Input
2	CLK	SPI Serial Clock Input
3	RST	SPI register reset, internal integrated 80 k Ω pull-down
4	LD_GPO	LD/GPO Output Port
5, 6	RF_INN, RF_INP	RF Signal Differential Input Port
7	VCC_RF	RF Divider Power Supply, 3.3 V
9	VCC_BIAS	Internal bias supply, 3.3 V supply
11	VCC_PD	Phase detector power supply, 3.3 V
16	CP	Charge pump output port
17	VCC_CP	Charge pump power supply, 3.3 V power supply
18	VCC_REF	Reference divider supply, 3.3 V
19	REF_IN	Reference clock REF input port
21	SDO	SPI Serial Data Output Port for SPI Cascade
22	VDD	Digital module power supply, 3.3 V power supply
23	CEN	Chip Enable Port, High Enable, Internally Integrated 80 k Ω Pull Up
24	LE	SPI serial-parallel conversion control signal, rising edge triggers serial data write. Internal integrated 80 k Ω pull-up
8, 10, 12 ~ 15, 20	NC	NC Suspended
Chip back	GND	Ground port

Chengdu Cuiwei Electronic Co.,LTD
Address: No. 5, Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

SPI Control Description

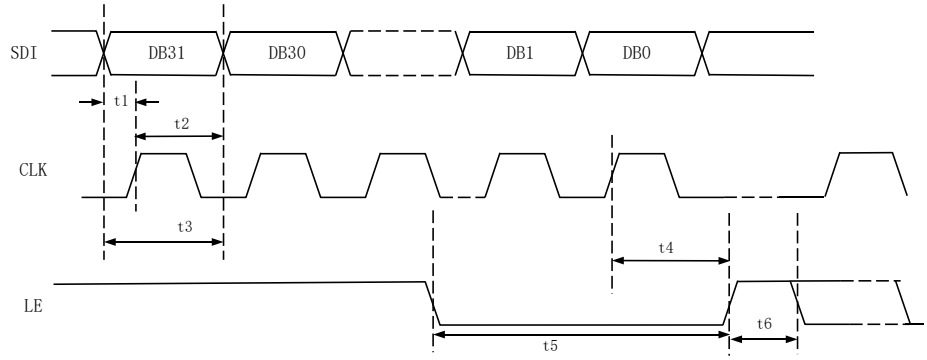
Timing requirements:

Parameter	Minimum value	Maximum value	Description
t1	5n		data setup time
t2	5n		data hold time
t3	20n		data (clk) period
t4	10n		Setup time from clk rising edge to LE rising edge
t5	10n		Time from falling edge of LE to next rising edge of LE
t6	5n		LE High Width

SPI Register Bit Description:

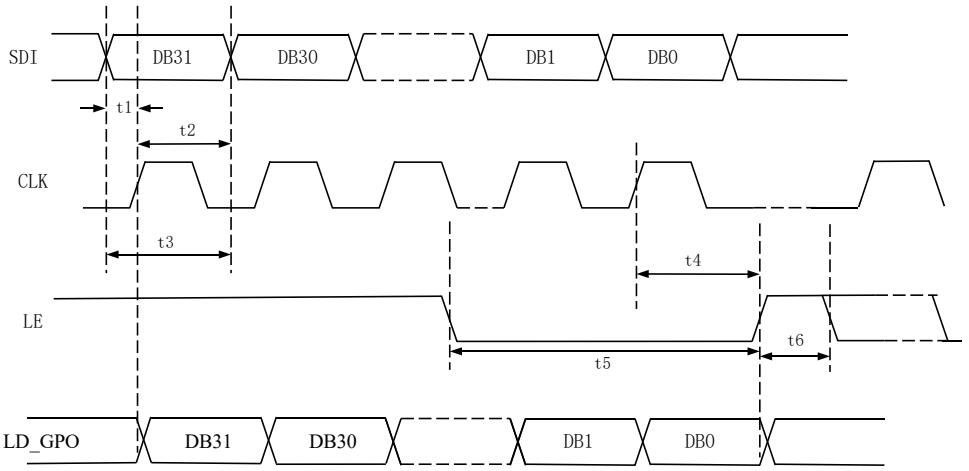
DB31 ~ DB8	DB7 ~ DB3	DB2 ~ DB0
SPI input data bits DIN < 23 > ~ DIN < 0 >	SPI Register Address Bits AD < 4 > ~ AD < 0 >	Chip identification bit CA < 2 > ~ CA < 0 >

Write cycle timing:



a. The host places 24-bit data d23: d0 (MSB first) on the SDI on the first 24 falling edges of the CLK.
b. The slave moves data on SDI on the first 24 rising edges of CLK.
c. The 5-bit register address r4: r0 (MSB first) to be written by the host is placed on the next 5 falling edges (25-29) of CLK.
d. The slave moves in register bits on the next five rising edges (25-29) of CLK.
e. The host places the 3-bit chip address a2: a0 (MSB first) on the next 3 falling edges (30-32) of the CLK.
f. The slave moves in the chip address on the next three rising edges (30-32) of CLK.
g. The host sets LE after the 32nd rising edge of CLK.
h. The slave moves SDI data to the specified register on the rising edge of LE.

Read cycle timing:



A. bit [4: 0] of address 00h is written according to the writing cycle timing;

b. Read back the value of the corresponding register according to the value of the address 00h;

c. The first 8 clk values are read back to 0, and the next 24 clk values are actually read out

Register description:

Address bit hexadecimal	Bit number	Type (read/write)	Register name	Bit width	Default value	Description
Read address register						
00h	4: 0	WR	read address	5	0	Address when SPI reads data
Logic control register						
01h	0	WR	PD_ALL	1	0	Global shutdown control
	1	WR	BLK_UVLO	1	0	Masking UVLO signals
REF Register						
02h	13: 0	WR	rdiv	14	1	REF sub-frequency, 14 bits
	14	WR	PD_REF	1	0	Forced shutdown of REF divider
Integer frequency division register						
03h	18: 0	WR	intg	19	'h3c	RF integer division, 19 bits
	19	WR	div2	1	0	RF Input Divide 2 Enable
	20	WR	PD_RF	1	0	Forced shutdown of RF divider
Fractional frequency division register						
04h	23: 0	WR	frac	24	0	RF Fractional Fractional Frequency, 24-bit

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Address: No. 5, Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

SPI Control Description

Register description (continued):

Address bit hexadecimal	Bit number	Type (read/write)	Register name	Bit width	Default value	Description
DSM control register						
06h	0	WR	n_reset	1	1	Reset signal, low active, reset for one REF period and return to 1
	1	WR	n_intrp	1	1	Reset signal, low active, reset for one REF period and return to 1
	2	WR	mash_en	1	1	MASH1-1-1
	3	WR	fast_en	1	0	
	4	WR	order2_en	1	0	Single ring second order
	5	WR	int_en	1	0	Integer mode
	6	WR	dither_en	1	0	Self-dithering mode
	7	WR	lfsr_en	1	1	lfsr jitter mode
	8	WR	preset_en	1	0	Initial phase write enabled
	9	WR	preset_trig	1	1	Initial phase rising edge trigger
DSM preset register						
07h	23: 0	WR	Pre-set_phase < 23: 0 >	24	'h64	Initial phase value
Sweep control register						
08h	15: 0	WR	lock_cycles < 15:	16	'h258	
	16	WR	n_reset	1	1	Reset signal, low active, reset for one REF period and return to 1
	17	WR	swp_en	1	0	Sweep enabled, when effective, the integer and fractional frequency fractions of sweep output are forced Assign a value to the frequency divider
	18	WR	swp_trig	1	0	Trigger pulse, the rising edge is effective, and the recommended pulse width is 5ns
	21:20	WR	swp_mode < 1: 0 >	2	0	
	23:22	WR	force_lock < 1: 0 >	2	1	Frequency sweep controller inputs lock control: 0 or 1: LD output control lock 2: Force lock to 0 (unlocked state) 3: Force lock to 1 (locked state)
Sweep starting point integer frequency division register						
09h	18: 0	WR	nint_str < 18: 0 >	19	'h46	Sweeper starting point integer frequency division, 19 bits
Sweep starting point fractional frequency division register						
0Ah	23: 0	WR	nfrac_str < 23: 0 >	24	'hc8	Fractional frequency division at the starting point of frequency sweeper, 24 bits
Sweep end integer frequency division register						
0Bh	18: 0	WR	nint_trm < 18: 0 >	19	'h50	Sweeper end integer division, 19 bits
Sweep starting point fractional frequency division register						
0Ch	23: 0	WR	nfrac_trm < 23: 0 >	24	'h64	Sweeper end integer division, 24 bits
Sweep step register						
0Dh	23: 0	WR	step_swp < 23: 0 >	24	'h64	Sweep step control, 24-bit

SPI Control Description

Register description (continued):

Address bit hexadecimal	Bit number	Type (read/write)	Register name	Bit width	Default value	Description
Sweep integer frequency division output register						
0Eh	18: 0	RO	nint_out < 18: 0 >	19	0	Integer frequency division output of frequency sweeper, 19 bits, read directly when swp_en is invalid Output the integer frequency division value of DSM, that is, 03d < 18: 0 >
	19	RO	swp_busy	1	0	Sweep state indication
Sweep integer frequency division output register						
0Fh	23: 0	RO	nfrac_out < 23: 0 >	24	0	Fractional frequency division output of frequency sweeper, 24 bits, read directly when swp_en is invalid Output the fractional frequency division value of DSM, that is, 04d < 23: 0 >
LD/GPO register						
10h	2: 0	WR	LD Windows < 2: 0 >	3	0	LD decision window size, 0: 2ns 1: 5.5 ns 2: 11ns 3: 21ns 4: 30ns 5: 58ns 6: 114ns 7: 224ns
	4: 3	WR	LD wincnt < 1: 0 >	2	0	The LD window determines the count value, and the number of times the PFD is in the window reaches the set value Post-LD judgment is valid: 0: 64 1: 256 2:10 24 3:40 96
	5	WR	LD MODE	1	0	LD Mode: 0: PFD Delay Window Mode 1: PFD duty cycle mode
	6	WR	PD_LD	1	0	Forced shutdown of LD
	10: 8	WR	LD DCC < 2: 0 >	3	0	LD Duty Cycle Determination Range: 0:10% 1:15% 2:20% 3:25% 4:30% 5:35% 6:40% 7:45%

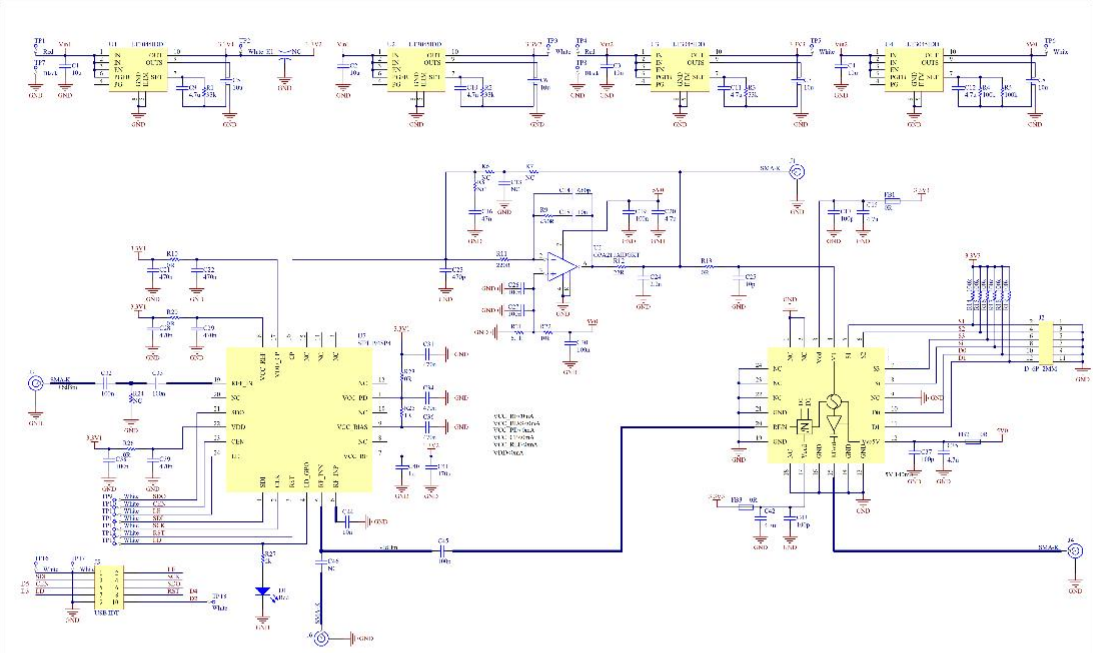
Chengdu Cuiwei Electronic Co.,LTD
Address: No. 5, Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

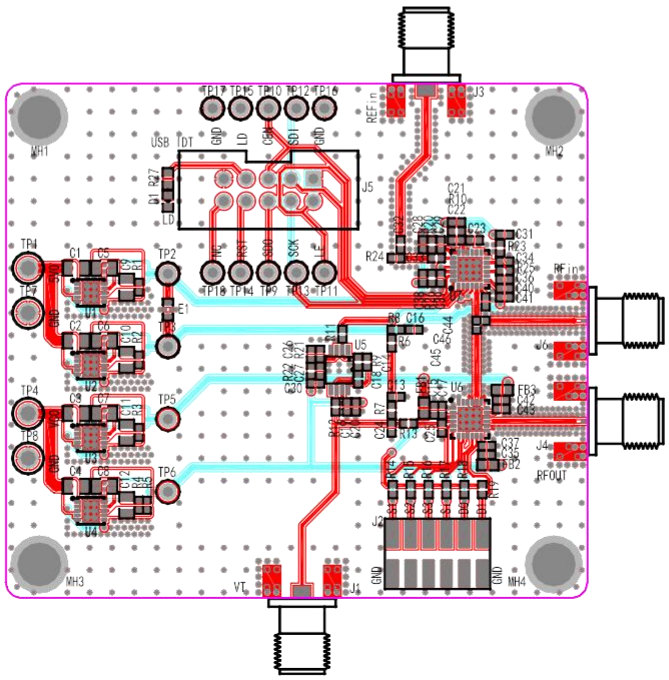
SPI Control Description

Register description (continued):

Address bit hexadecimal	Bit number	Type (read/write)	Register name	Bit width	Default value	Description
10h	19:16	WR	GPO < 3: 0 >	4	0	GPO Output Selection: 0: NC 1: REF_DIV 2: RF_DIV 3: UP 4: DN 5: VCP_mir1 6: VCP_mir2 7: VUVLO 8 ~ 15: NC
	23	WR	GPO_EN	1	0	Whether GPO is turned on or not, the LD port is changed to GPO mode after it is turned on 0: Turn off; 1: Open
PFDCP Register 1						
11h	1: 0	WR	PD tdelay	2	0	PFD reset delay: 0: 0.6 ns 1: 1ns 2: 1.4 ns 3: 1.8 ns
	2	WR	POL INV	1	1	PFD Polarity Control: 0: Polarity Normal 1: Polarity reversal
	4	WR	PD PFD	1	0	Forced shutdown of PFD
	5	WR	FUP CP	1	0	Valid only when PFD is shut down 0: Forcibly shut down the UP output of PFD 1: Force the UP output of the PFD,
	6	WR	FDN_CP	1	0	Valid only when PFD is shut down 0: Forcibly shut down the DN output of the PFD 1: Force the DN output of the PFD,
	15: 8	WR	CPGup	8	FF	CP gain current UP control word 20uA/ bit
	23:16	WR	CPGdn	8	FF	CP Gain Current DN Control Word 20uA/ bit
PFDCP Register 2						
12h	6: 0	WR	CPOS cur-	7	0	CP Compensation Current Control Word 5uA/bit
	7	WR	PD_CP	1	0	Forcibly shut down CP
	8	WR	CPOS UP EN	1	0	CP UP Compensation Current Enable
	9	WR	CPOS DN EN	1	0	CP DN Compensation Current Enable
	10	WR	PD_BIAS	1	0	Forcibly turn off BIAS current

Evaluation board circuit diagram





Evaluation Board Circuit Diagram (BOM List)

#	Designator	Comment	Description	Footprint	Manufacturer	Part Number	SOB	Quantity
1	!PCB1	PCB	Printed Circuit Board		Si_Core	EVAL-SIPL4SP4-B	Y	1
2	C1, C2, C3, C4, C5, C6, C7, C8	10u	Capacitor	0805, 0805_4	TDK	C2012X5R1E106K125AB	Y	8
3	C9, C10, C11, C12	4.7u	Capacitor	0805	TDK	C2012X5R1E475K125AB	Y	4
4	C13, C46	NC	Capacitor	0402	Murata	GRM155R71H104KE14D	N	2
5	C14	680p	Capacitor	0402	Murata	GCM155R71H681JA37D	Y	1
6	C15, C20, C35, C42	4.7u	Capacitor	0402	TDK	C1005X5R1A475K050BC	Y	4
7	C16	47n	Capacitor	0402	Murata	GRM155R71C473KA01D	Y	1
8	C17, C37, C43, C45	100p	Capacitor	0402	Murata	GRM1555C1H101FA01D	Y	4
9	C18, C44	10n	Capacitor	0402	Murata	GRM155R71H103JA88D	Y	2
10	C19, C26, C27, C30, C32, C33, C38	100n	Capacitor	0402	Murata	GRM155R71H104KE14D	Y	7
11	C21, C22, C28, C29, C31, C34, C36, C39, C41	470n	Capacitor	0402	Murata	GRM155R61A474KE15D	Y	9
12	C23	470p	Capacitor	0402	Murata	GCM1555C1H471JA16D	Y	1
13	C24	2.2n	Capacitor	0402	Murata	GCM155R71H222JA37D	Y	1
14	C25	10p	Capacitor	0402	Murata	GRM1555C1H100FA01D	Y	1
15	C40	1n	Capacitor	0402	Murata	GRM1555C1H102JA01D	Y	1
16	D1	Red	LED	0603D	WE	150060SS75003	Y	1
17	E1	NC	EMI Filter	NFM18C	Murata	NFM18CC223R1C3	N	1
18	FB1, FB2, FB3	0R	Resistor	0603	Yageo	RC0603JR-070RL	Y	3
19	J1, J3, J4, J6	SMA-K	RF Connecter	SMA_40G, SMA_DC	傲文	D550B12E01-023	Y	4
20	J2	D_6P_2MM	HEADER	D_6P_2MM	Harwin	M22-5320605	Y	1
21	J5	USB IDT	Header, 5-Pin, Dual row	IDC2.54-10		DC3-10P	Y	1
22	MH1, MH2, MH3, MH4	702932000		702932000	WE	702932000	Y	4
23	R1, R2, R3	33k	Resistor	0402	Yageo	RC0402FR-0733KL	Y	3
24	R4, R5, R14, R15, R16, R17, R18, R19	100k	Resistor	0402	Yageo	RC0402FR-07100KL	Y	8
25	R6	NC	Resistor	0402	Yageo	RC0402FR-07750RL	N	1
26	R7	NC	Resistor	0402	Yageo	RC0402JR-070RL	N	1
27	R8	NC	Resistor	0402	Yageo	RC0402FR-07300RL	N	1
28	R9	430R	Resistor	0402	Yageo	RC0402FR-07430RL	Y	1
29	R10, R13, R20, R23, R26	0R	Resistor	0402	Yageo	RC0402JR-070RL	Y	5
30	R11	220R	Resistor	0402	Yageo	RC0402FR-07220RL	Y	1
31	R12	22R	Resistor	0402	Yageo	RC0402FR-0722RL	Y	1
32	R21	5.1k	Resistor	0402	Yageo	RC0402FR-075K1L	Y	1
33	R22	10k	Resistor	0402	Yageo	RC0402FR-0710KL	Y	1
34	R24	NC	Resistor	0402	Yageo	RC0402FR-07100RL	N	1
35	R25	1R	Resistor	0402	Yageo	RC0402FR-071RL	Y	1
36	R27	2k	Resistor	0603	Yageo	RC0603FR-072KL	Y	1
37	TP1, TP4	Red	Test Point	Keystone5005	Keystone	Keystone5005	Y	2
38	TP2, TP3, TP5, TP6	White	Test Point	Keystone5002	Keystone	Keystone5002	N	4
39	TP7, TP8	Black	Test Point	Keystone5006	Keystone	Keystone5006	Y	2
40	TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18	White	Test Point	Keystone5002	Keystone	Keystone5002	Y	10
41	U1, U2, U3, U4	LT3045IDD	LDO	DFN10	ADI	LT3045IDD	Y	4
42	U5	OPA211AIDGKT	Operational Amplifier	MSOP8	TI	OPA211AIDGKR	Y	1
43	U6	SIV100SP4	VCO	SP4	Si_Core	SIV100SP4	Y	1
44	U7	SIPL194SP4	PLL	SP4	Si_Core	SIPL194SP4	Y	1

Chengdu Cuiwei Electronic Co.,LTD
Address: No. 5, Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com